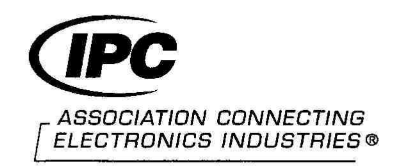


IPC-D-279

Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies

Developed by the SMT Design Reliability Task Group (6-10b) of the Product Reliability Committee (6-10) of IPC

Users of this standard are encouraged to participate in the development of future revisions.

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Acknowledgment

Any Standard involving a complex technology draws material from a vast number of sources. While the principal members of the SMT Design Reliability Task Group of the Product Reliability Committee are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

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Vern Solberg, Tessera
Werner Engelmaier, Engelmaier Associates

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Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies

1.0 SCOPE

This document establishes design concepts, guidelines, and procedures intended to promote appropriate 'Design for Reliability (DfR)' procedures and to ensure reliable printed wiring assembly (PWA) characteristics. The major focus of the information presented is directed toward those PWAs that have surface mount (SM) components, either totally, or intermixed with through-hole components, mounted on one or both sides of the mounting structure.

1.1 Purpose The definition of reliability in this document is:

> *Reliability* is the ability of a product to function under given conditions and for a specified period of time without exceeding acceptable failure levels.

This document addresses reliability-related aspects of product design, process design, as well as material/component selection and qualification. This document identifies appropriate existing IPC documents for basic detailed information.

The effort of this document is directed at SMT; the interconnect structure and the solder joint will receive most of our attention.

1.2 Design Philosophy Before the product design effort can begin, the designers of the product and assembly process need to know the customer's reliability requirements for the product. These requirements should be defined and ranked by a concurrent engineering or cross-functional team through a process such as Quality Function Deployment (QFD), used to capture the voice of the customer.

1.2.1 Establishing the Design Team The design team can include but is not limited to the members who participate in at least the design activities identified in Table 1-1. In this table, DfA/M stands for Design for Assembly/Manufacturability, DfT for Design for Testability, DfR for Design for Reliability.

The design team can consider the general design guidelines and issues presented in the body of this document as a methodology for achieving its reliability goals. Figure 1-1 illustrates the general design steps and process flow using concurrent engineering. Figure 1-2 illustrates the interactive nature of the design for reliability process.

1.2.2 Defining Reliability Requirements The basic reliability requirements to be defined include:

Table 1-1 The Design Team

Design/Engineering Function		Team Inprovement Area		
Product	(QFD)	(DfA/M)	(DfT)	(DfR)
Circuit	(QFD)	(DfA/M)	(DfT)	
Printed board		(DfA/M)	(DfT)	(DfR)
Thermal	(QFD)			(DfR)
EMC, EMI, ESD	(QFD)		(DfT)	(DfR)
Mechanical	(QFD)	(DfA/M)	(DfT)	(DfR)
Software	(QFD)		(DfT)	
Marketing	(QFD)			
Process/ manufacturing	(QFD)	(DfA/M)		
Test	(QFD)		(DfT)	(DfR)
Package/component		DfA/M)	(DfT)	
Field Service	(QFD)		(DfT)	
Purchasing		(DfA/M)		
Material	(QFD)	(DfA/M)	(DfT)	(DfR)
Reliability	(QFD)	(DfA/M)	(DfT)	(DfR)
Regulations	(QFD)		(DfT)	
Upper management	(QFD)	Conceptual Design and Cultural Change		

- years of service
- acceptable failure rate(s)/probability(ies) as a function of time
- repair/replacement/upgrade/service/maintenance/warranty strategy
- life cycle environment(s)
- definition of acceptable performance
- criticality of function(s)
- available test equipment

1.2.3 Understanding the Product Life Cycle The life cycle begins at the component level (including the printed board) and continues through the assembly level; the life cycle includes exposure to the following environments:

- assembly/process
- testing
- storage
- transportation
- operating

Test, storage and transportation need to be considered at both component and assembly levels as well as before, during, and after the assembly process.

1.2.4 Defining the Product Environment For each environment, in 1.2.3, it is critical to identify, characterize and quantify the parameters listed below:

- Temperature Range
- Time at Temperature
- Temperature Rate of Change
- Kind and number of temperature cycles
- Duty Cycle
- Humidity (moisture) exposure
- Atmospheric pressure conditions (earth, space, both)
- Vibration and shock
- ESD, EOS, EMC, EMI and high voltage exposures and requirements
- Chemical exposures (flux, solvents, salt spray, NBC, decontamination, etc.)
- Radiation (Ionizing, light, UV)
- Contamination (dust, oil, paper)
- Pressure conditions

When the life environments have been identified and defined, the engineering team is prepared to analyze and select the materials, components, assembly processes, thermal management and test strategies required.

1.3 Document Organization This document has been organized to provide the reader with consistent information on the various aspects of surface mount technology printed board assemblies and identifies the parameters that need to be addressed. Each section serves a specific function in the SMT design process. The body of this document addresses general design guidelines specific to SMT. The appendices contain detailed information of SMT design or common design considerations between SMT and through hole processes.

1.3.1 Applicable Documents Section 2.0 lists only those documents related to surface mount technology and reliability which are mentioned in the text. The design engineers need to know about the primary documents which underlie the text. The bibliography, Section 9, lists documents by interest area and some entries are duplicated; there are many more documents of use and available to the designer. This lists only those documents used day to day.

1.3.2 Design for Reliability of SM Assemblies Section 3.0, together with Sections 4.0 and 5.0, considers the broad range of environmental stresses to which the printed wiring assembly (PWA) must be robust during its life cycle (life cycle environment) and some specific mitigation techniques that may be used. A separate Appendix D for SM thermal design augments Appendix A for the DfR of solder attachments and Appendix B for DfR of plated-through vias (PTVs). Appendix C provides DfR information for insulation resistance aspects. Appendix E provides DfR information for insulation resistance aspects Appendix E relates environmental stresses and the corresponding PWA and component responses. Appendix G provides material CTE data. Appendix I describes solvent related stresses on plastics and metals. Appendix L deals with corrosion. Appendix M discusses solder joint variability. Appendix N deals with adhesives, solder masks and conformal coatings. Appendix O covers the special requirements for high altitude and aerospace applications.

1.3.3 Substrates Section 4.0 covers rigid and flexible substrates and their impact on SM assembly reliability. Data on material parameters and tradeoffs is provided. Substrate related issues such as thermal expansion mismatch, moisture absorption, and PTH-via thermal stress are covered. Related materials CTE data is provided in Appendix G. Appendix N deals with adhesives, solder masks and conformal coatings. A detailed DfR treatment for PTVs is provided in Appendix B.

1.3.4 Components Section 5.0 covers components, component-related design issues, and component-process interactions of concern to the designer as well as to the process engineer. Appendix E relates environmental stresses and the corresponding PWA and component responses. Appendix F provides a ready reference to surface mount plastic package cracking during SM reflow and to methods for mitigating those effects. Appendix H provides a ready reference to the electrostatic discharge susceptibility groupings of various component families.

1.3.5 Attachment Materials and Coatings Section 6.0 addresses attachment materials and polymer coatings. The attachment materials include solder, electrically conductive adhesives, thermally conductive adhesives and structural adhesives. The polymer coatings include solder mask conformal coating.

1.3.6 Assembly Processes and DfM Section 7.0 provides an overview of the assembly processes used in surface mount assemblies and highlights the specific reliability issues associated with each of the individual processes, including design for manufacturability (DfM) considerations. The surface mount processing conditions may be the most severe that the assembly ever sees during its life cycle, not only in terms of temperature but shock and flexure as well. A DfM checklist is provided listed in Appendix K together with pointers to DfM assessment tools in software. A detailed list of solvent/plastic/metal compatibilities is provided in Appendix I.

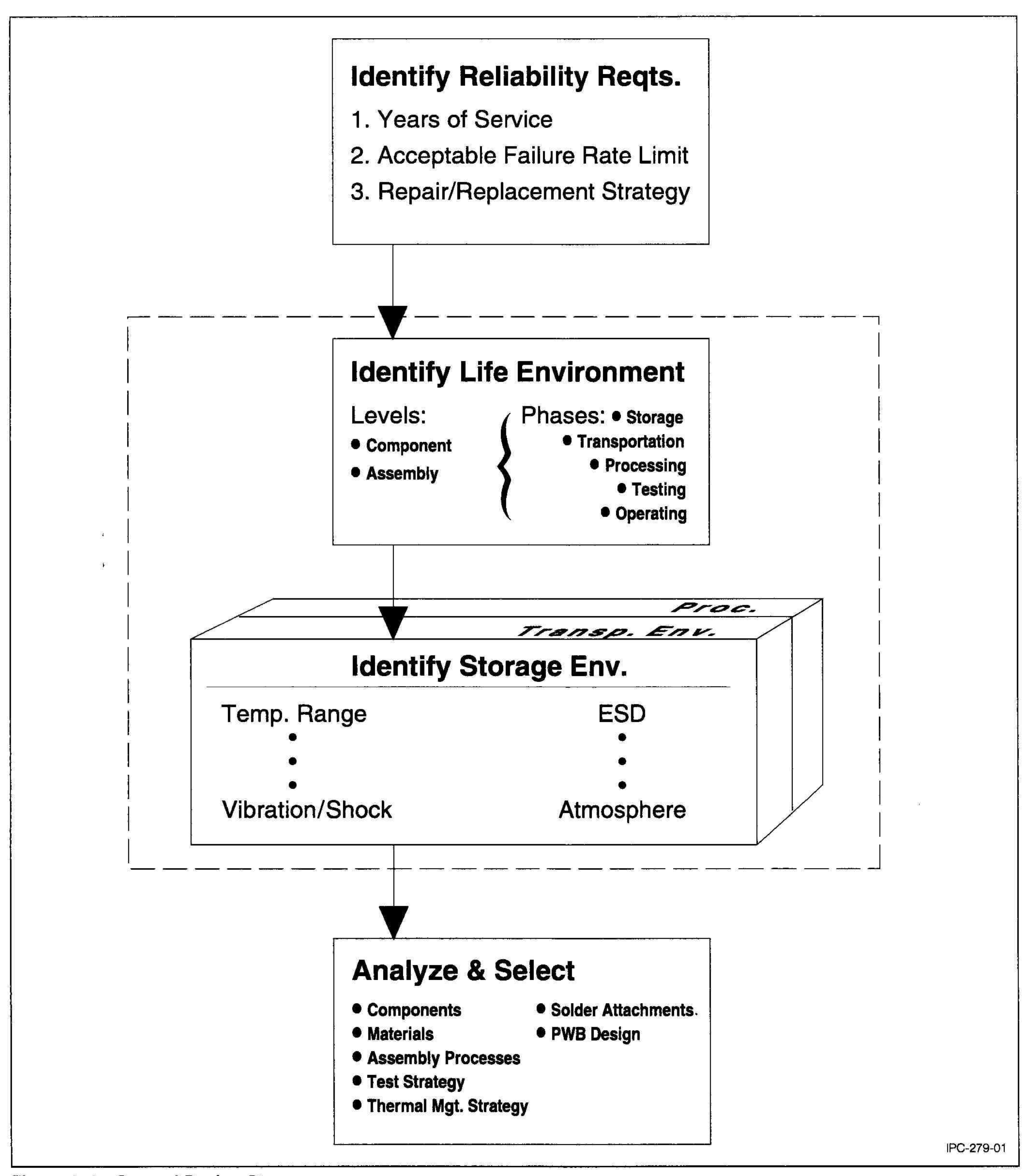


Figure 1–1 General Design Steps

1.3.7 Testing Section 8.0 details the various testing strategies, their purposes and their impact on reliability. Also discussed are design for testability considerations. Checklists for DfT from various sources are provided in Appendix J.

1.4 Terms and Definitions Terms and definitions used here are in accordance with IPC-T-50, and IPC-SM-785 except as otherwise specified.

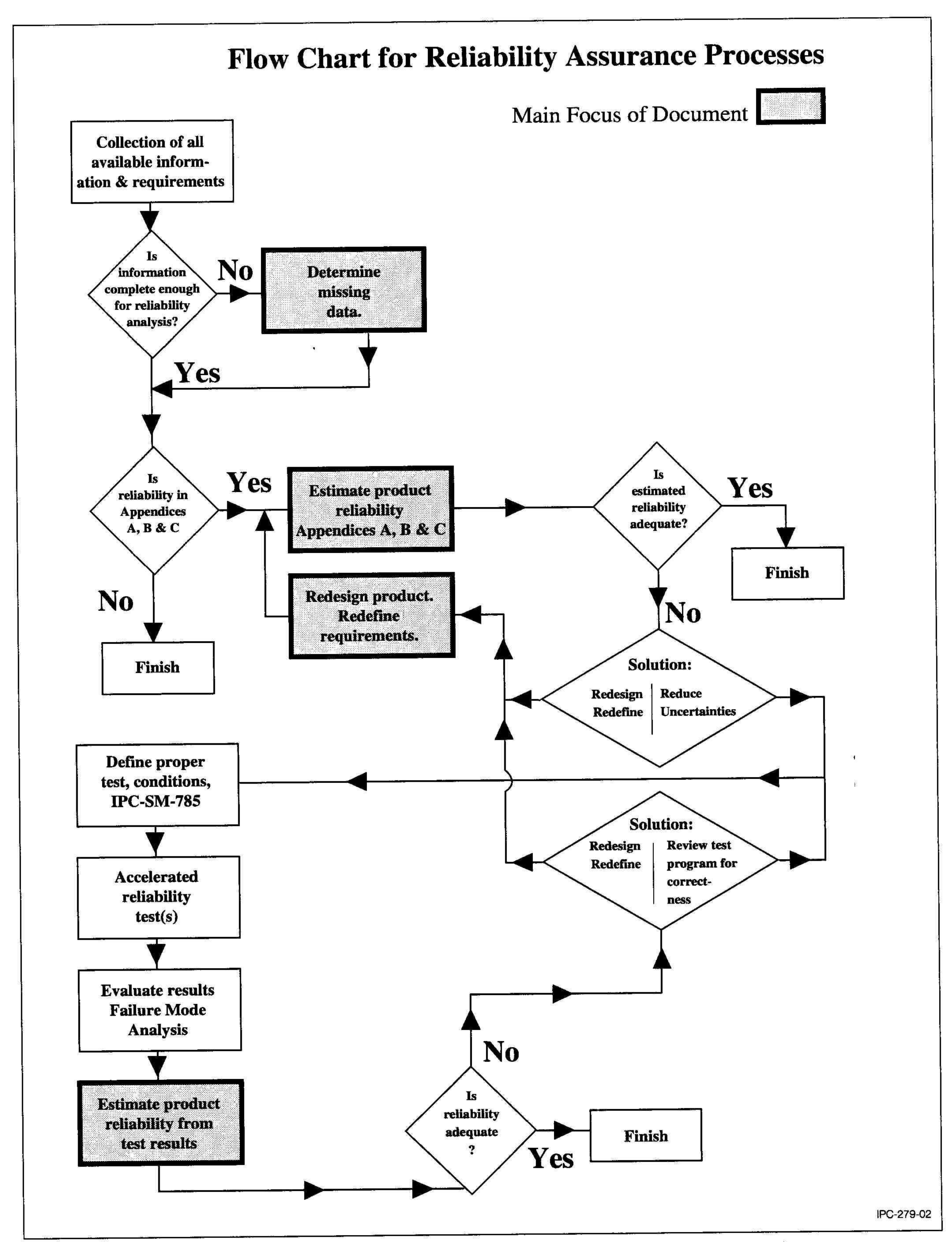


Figure 1-2 Flow Chart for Reliability Assurance Processes

2.0 APPLICABLE DOCUMENTS

The following documents of the issue in effect on the date of issuance of this specification, form a part of this specification to the extent specified herein. Subsequent issues of, or amendments to, these documents may become a part of this specification.

2.1 Institute for Interconnecting and Packaging Electronic Circuits (IPC)[1]

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-D-275 Design Standard for Rigid Printed Boards and Rigid Printed Board Assemblies

IPC-TR-476 How to Prevent Electrically Induced Failures (Electromigration) in Printed Wiring Board Assemblies

IPC-TM-650 Test Methods Manual

2.6.20 Assessment of Plastic Surface Mount Components for Susceptibility to Moisture Induced Damage

IPC-ET-652 Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards

IPC-PE-740 Troubleshooting guide for Printed Board Manufacture and Assesmbly

IPC-SM-782 Surface Mount Design and Land Pattern Standard

IPC-SM-785 Guidelines for Accelerated Surface Mount Solder Attachment Reliability Testing

IPC-SM-786 Procedures for Characterizing and Handling of Moisture/Reflow Sensitive ICs

IPC-SM-816 SMT Process Guideline and Checklist

2.2 Electronic Industries Association[2]

EIA-541 Packaging Material Standards for ESD Sensitive Items

EIA-583 Packaging Material Standards for Moisture Sensitive Items

EIA-625 Requirements for Handling Electrostatic Discharge Sensitive (ESD) Devices

JESD 22-A112 Moisture-Induced Stress Sensitivity for Plastic Surface Mount Devices

JESD 22-A113 Preconditioning Procedures of Plastic Surface Mount Devices Prior to Reliability Testing

JESD 42 Requirements for Handling Electrostatic-Discharge Sensitive (ESDS) Devices

JEP113 Symbol and Labels for Moisture Sensitive Devices

2.3 Joint Industry Standards

J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies

J-STD-004 Requirements for Soldering Fluxes

3.0 DESIGN FOR RELIABILITY FOR SURFACE MOUNT ASSEMBLIES

During the initial design stages of any project, a full knowledge of the product requirements must be understood. These requirements include the life cycle environment, printed board design constraints, thermal effects, serviceability, and all aspects of reliability. This section reviews these considerations and the effects caused by each. The design details for DfR are discussed in Appendices A, B, and C.

3.1 Life Cycle Environment The environmental influences that determine the reliability of surface mount assemblies have to include all environments from manufacture to the end of the design life. These life cycle environments include manufacturing processes, burn-in and/or ESS procedures, transport, storage and use conditions.

Depending upon the product application, any of the life cycle environment periods may have an overwhelming effect on the product reliability. The effects of all these life cycle environment periods can accumulate and need to be summed together using the Palmgren-Miner's rule. (See Equations #9 through #11 in Appendix A)

3.1.1 Manufacturing Processes Many manufacturing processes used in Surface Mount Assembly require changes in temperature. The most severe of these are processes requiring the melting of solder. These processes can affect PTH and PTVs, solder attachments, components and printed boards. Other processes include bake-out of printed boards, curing of adhesives, and curing of polymeric coatings.

3.1.2 Processing Temperature Excursions During processing and assembly of electronic assemblies, temperature excursions, particularly during solder reflow and repair, cleaning, or imposed thermal cyclic testing, take place that are damaging to some parts of the assemblies and consume part of the available life. These thermal excursions can cause fractures in the PTVs of the multilayer printed board.

1. IPC, 2215 Sanders Road, Northbrook, IL 60062-6135.
2. Electronic Industries Association, 2001 Eye Street, N.W., Washington, DC 20006.

Table 3–1 Realistic Representative[1] Use Environments, Service Lives, and Acceptable Failure Probabilities for Surface Mounted Electronics Attachments by Use Categories

	Worst-Case Environment						
Use Category	Tmin °C	Tmax °C	ΔT[2] °C	Dwell Time t_D hrs	Cycles/Year	Typical Years of Service	Accept. Failure Risk[3], %
Consumer	0	+60	35	12	365	1-3	~1
Computers	+15	+60	20	2	1460	~5	~0.1
Telecom	-40	+85	35	12	365	7-20	~0.01
Commercial Aircraft	-55	+95	20	12	365	~20	~0.001
Industrial and Automotive Passenger Compartment	–55	+96	20 &40 &60 &80	12 12 12 12	185 100 60 20	~10	~0.1
Military Grounds and Ship	–55	+95	40 &60	12 12	100 265	~10	~0.1
Space leo geo	–55	+95	3 to 100	1 12	8760 365	5-30	~0.001
Military Avionics a b c Maintenance	–55	+95	40 60 80 &20	2 2 2 1	365 365 365 365	~10	~0.01
Automotive under hood	–55	+125	60 &100 &140	1 1 2	1000 300 40	~5	~0.1

& = in addition
1 Does not cover all possible use environments, but only most common.
2 ΔT represents the maximum temperature swing, but does not include power dissipation effects for components; for reliability estimations the actual local temperature swings for components and substrate, including power dissipation should be used.
3 The 'Acceptable Failure Risk' is the percentage of product in the field that has failed, due to wearout mechanisms, at the end of the 'Typical Years of Service.'

This damage should be minimized by keeping the number of excursions to a minimum; and the damage needs to be considered in the overall reliability estimates for the assemblies. See IPC-PE-740 for trouble-shooting information.

3.1.3 Burn-In and Environmental Stress Screening (ESS) Burn-in tests and ESS have the potential of identifying latent defects that may cause early failures in product, but they also have a negative impact on the good assemblies. The degree of the detrimental impact on reliability depends on the severity of the burn-in and/or ESS procedures.

Burn-in testing generally should be a complete environmental test involving perhaps worst case but still realistic operational environments.

ESS should never be employed routinely. ESS needs to be specifically designed to cause the failure of "weak" elements in the assemblies for which a strong suspicion of processing defects exists.

The assembly elements that are typically most affected by these procedures are the surface mount solder attachments. The effect of extended solder joint temperature cycling can use up a significant amount of solder joint life.

3.1.4 Transport While transport conditions like vibration, mechanical shock and moisture are routinely considered and accommodated, little is done about the thermal conditions. Electronic product can sit on loading docks or in warehouses, or be in cargo holds of ships, airplanes and/or trucks, in temperatures ranging from –40 to +70°C.

For some applications, e.g. medical implants, these transport conditions would be significantly more severe than the operational environments.

3.1.5 Storage For some product applications, the environmental conditions during storage become significant in the total life cycle environment. In particular, military applications, such as munitions (proximity fuses, etc.), and space applications can require long storage periods, frequently in uncontrolled environments, before final use.

The user should consult with the vendor to determine the shelf life and special storage conditions.

3.1.6 Use Environments The use environments are highly dependent upon the product application. In Table 3-1, typical worst case use environments for 9 product categories are given. These use environments should be regarded as guidelines only; the actual use environment as well as the environmental conditions of the SM assembly being designed may be significantly different.

3.1.7 Environmental Stresses The operating life of a surface mounted assembly is dependent upon a number of factors which include intended usage, usage environments, strength of the materials and components to withstand the stresses imposed by the usage and the environments, material (variables), etc. In a surface mounted assembly, the most critical element from the life cycle viewpoint are the solder joints and PTVs. Cyclic (or fatigue) displacements experienced during various phases of the product's life cycle are responsible for consumption of useful life of material elements.

One of the major contributors to the cyclic loading is thermal cycling due to the internal power cycling and external environmental changes. Another important contributor is vibration during the operational use, transportation, handling, etc. An estimate of the fatigue life of the solder assembly that will be consumed by these fatigue cycles during the product's life cycle can be obtained by performing a cumulative damage analysis.

It should be noted that the cumulative damage analysis requires the knowledge of fatigue characteristics of the materials involved. Also, a thorough understanding of how the product will be used, handled and maintained, by the user and under what environments, is necessary. See Appendix E.

3.1.8 Temperature/Thermal Temperature is one of the most important parameters in the use environment that must be considered in the SM PWA design process. Temperature history is the most significant parameter affecting the reliability of SM solder joints. For some product applications, the use environment consumes the most significant portions of the required fatigue life; this is typically the case where the product development cycle includes producing a prototype prior to the "final build."

Therefore, DfR depends to a large extent on the thermal design for the assembly, as well as the external thermal environment. Temperature is also important, since many materials in electronic assemblies have properties which change significantly with temperature.

3.1.9 Cyclic Temperature Swings Cyclic thermal excursions, ΔT, cause thermal expansion mismatches due to different parts of the assemblies having materials with different CTEs and/or being at different temperatures. Thus, the size of the cyclic temperature swing is proportional to the resulting loading. The larger the ΔT, the larger the threat to reliability.

During cyclic temperature excursions, these cycles can have different profiles, e.g., sinusoidal, trapezoidal, sawtooth, square-wave, etc. These differences are important in understanding time-dependent and rate-dependent processes. The transient parts of the profile give the ramping rates of the temperature change which can cause transient temperature gradients and over-stress conditions. The steady-state, or near steady-state, parts of the profile determine the duration of the temperature dwells which are important for time-dependent processes like creep and stress relaxation.

3.1.10 Thermal Shock In thermal shock, the extremely rapid temperature changes (~30°C/minute and above) result in warping of the surface mount assembly. The warpage is caused by large transient thermal gradients induced by the rapid temperature change when the boards are plunged into a new thermal environment. The warpages result in tensile and shear stresses where the tensile loading dominates over the steady state expansion mismatch. Thus, even assemblies with matched coefficients of thermal expansion will exhibit solder joint failures when subjected to thermal shock. The thermal shock loading mechanism is summarized in Figure 3-1.

Thermal shock conditions can arise from several sources. Examples of these are:

1) Rapid changes in external environment, e.g., sun-to-shade in space, missile launch, wing-mounted avionics, automobile start-up from very cold.
2) Rapid changes in power dissipation.
3) Various manufacturing/repair processes, e.g., reflow, vapor degrease, rework, etc.

The distinction between thermal shock and thermal cycling is not always addressed in designing reliability experiments. There is a fundamental difference between thermal shock and thermal cycling. The primary differences arise from the mechanism of loading. Thermal shock tends to result in multiaxial states of stress dominated by tensile overstresses and tensile fatigue. On the other hand, as previously discussed, thermal cycling results in shear loads and failure occurs from an interaction of shear fatigue and stress relaxation.

Thermal shock is usually performed in dual chamber arrangements or with liquid nitrogen injection whereas thermal cycling is performed in single chamber cycling equipment. Dual chamber arrangements will produce temperature transition rates in excess of 50°C/minute.

Single chambers generally do not produce transition rates even close to 30°C/minute which is the rate necessary to induce thermal shock. The results of these two types of testing are generally incompatible. Finally, thermal shock testing for purposes of evaluating surface mount solder joint reliability is only appropriate if thermal shock is indeed a field condition encountered by the product.

In some specifications, the definitions of thermal cycling and thermal shock are not fully differentiated; the rates of change are more closely associated with what we are calling thermal shock.

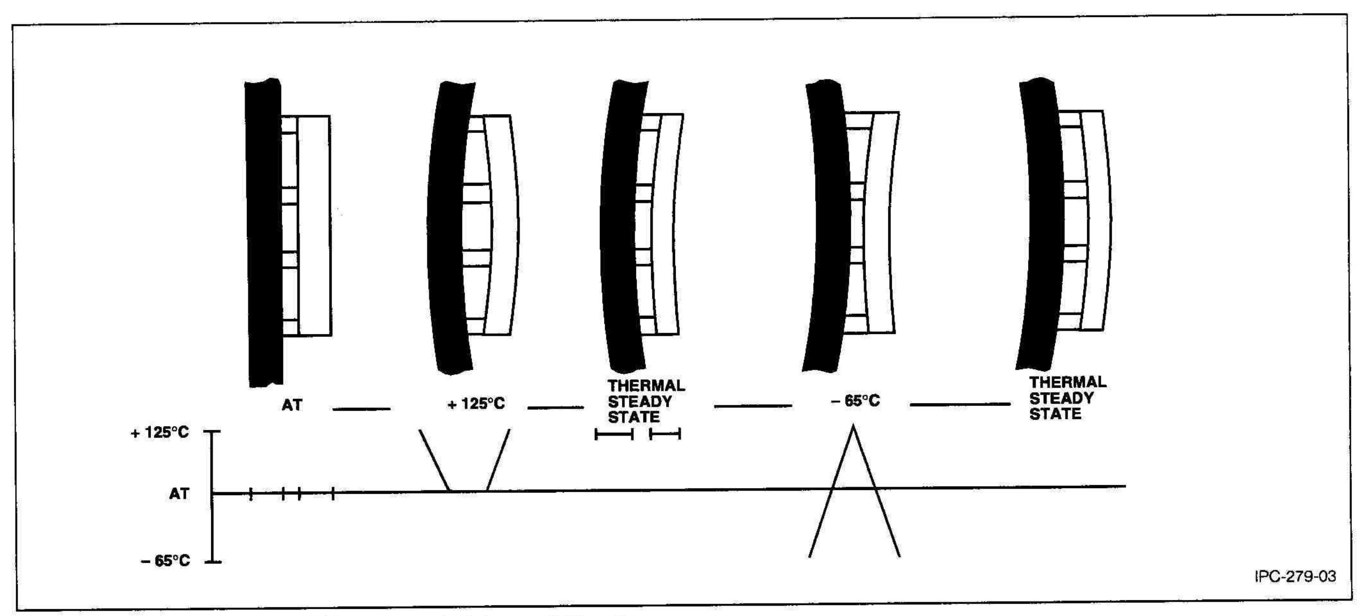


Figure 3–1 SMT Assembly Response to Thermal Shock

3.1.11 Electrical

3.1.11.1 ESD Susceptibility and Damage Prevention

All electronic components containing thin conducting or insulating films are susceptible to electrostatic discharge (ESD) damage. These components include those fabricated in high speed technologies (MOS, bipolar, GaAs), thin film technologies (resistors, integrated circuits, magnetic heads, MOS capacitors), and in future, wafer scale integration and multichip modules.

3.1.12 EMC/EMI The electromagnetic spectrum is usually divided into categories ranging from the long-wavelength radiation from power lines through radio, infrared, visible, ultraviolet, and x-rays, to gamma rays at the short-wave end. All electromagnetic waves consist of an electric field and a magnetic field. The relative magnitude of these fields depend on the emitter (EM source), wave propagation medium, and the proximity of the emitter to the subject assembly.

Many electronic circuits are susceptible to electromagnetic radiation and must be shielded to ensure proper operation. One of the most important effects of the electromagnetic radiation in the environment is electromagnetic interference (EMI). EMI is the electro-magnetic disturbances that impair the desired signal. In practice, EMI is often divided into two categories: conducted EMI and radiated EMI. Conducted EMI is an interfering signal resulting from an undesirable voltage or current coupled into a signal or other pertinent conductor. Radiated EMI is an interfering signal resulting from an electric and/or magnetic field amplitude and frequency spectra intentionally or unintentionally radiated by an electrical source. Examples of radiated emission sources are radio and TV transmitters, lightning, digital system noise from electronic control systems, etc. In military applications, an important effect is the interaction of electromagnetic radiation with electroexplosive devices used as detonators. Improper EMI could accidentally initiate the explosion.

EMC is the ability of electronic systems to operate in the intended electromagnetic environment at designed levels of performance and efficiency. The most direct approach to protection is, in most cases, to avoid the limited region in which high radiation levels are found. When exposure cannot be avoided, shielding is the important protective measure. The material selected for shielding can be an important factor. Ideal materials include steel, copper and nickel coating. In the design process, apertures for cooling ventilation and cable connections on the shielding box should be properly designed so that the EMI will have no influence inside the shielded space.

3.1.13 Mechanical Shock and Vibration Shock and vibration are common accelerators of failure in electronic packaging. The most frequent vibration-induced failures in surface mount are:

1. Flexing of leads and interconnects.
2. Dislodging or damaging of parts and structures.

Methods have been developed to counter the destructive effects of shock and vibration. Generally, isolation of a printed board against the effects of shock and vibration requires that the natural frequency of the printed board be substantially lower than the undesired frequency of vibration to avoid the resonance.

The basic system level isolators available are:

1. Natural or synthetic rubber, used to damp the vibration.

2. Metallic isolators including springs, metal meshes or wire rope; the latter provide smooth friction damping.

There are also other isolators such as viscous dampers which are velocity-sensitive. For high-frequency vibration, viscous dampers tend to become ineffective.

There are two approaches that may be taken when shock and vibration are present: either isolate the printed board or design it to withstand the shock and vibration. Studies have shown that the ideal goal is to design equipment to be resistant to shock and vibration, rather than to isolate it from these forces.

Because the surface mount components are generally smaller compared to the through-hole counterparts, they are more vibration resistant due to the lower inertia. As the PWA vibrates, the components mounted on the board are subject to stress from two different effects. First, the mass of the components is subjected to an acceleration that produces a force. The body of the component is kept in equilibrium with reactive forces developed in the leads. Second, the printed board flexes, which tends to bend the leads back and forth at their joints with the board. Because of the shorter lead lengths in SMT, the mechanical stress induced by shock and vibration in leads is considerably smaller compared to that in through-hole leads.

To detect/precipitate the flaws, stress screening with random vibration should be performed. Usually, stress screening should be designed so that it causes minimal damage to properly designed printed boards. This requires careful determination of the screening intensity.

Depending upon the applications, the frequency ranges are very different. For instance, the range for submarine electronic equipment is about 4-34 Hz, but for avionics the range is 15-2000 Hz.

The following considerations must be included in the analysis design for shock and vibration:

1. The location of the surface mount components relative to the supporting structure (i.e., edge, corner, or center of the supporting structure).
2. The orientation of the components with respect to the anticipated direction of the shock or vibration forces.
3. The maximum deflection of the printed board.

Mechanical shock to, and flexure of, a SM Printed Wiring Assembly can occur during its life cycle. Each incident could be characterized by the energy to be absorbed by the assembly, the shock peak amplitude, duration and time rate of change for correlation to sample shock testing:

- PWA struck by tooling during assembly (component insertion or placement, riveting, testing, test fixtures, probing, or depanelling)
- PWA installed into a card carrier or motherboard
- PWA dropped on a hard bench or floor
- Assembly dropped on a hard bench or floor
- Boxed product bounced and jolted during transportation
- Boxed product dropped on a hard bench, floor, truck bed
- Product (in use) dropped on a hard work surface or floor
- Product (in use) struck by passing equipment
- Product stored in racks, PWA fixtures, or rework station grips.
- PWA subjected to combined environmental stress in field use.

The assessment of the potential quality/reliability degradation of a printed wiring assembly (PWA) resulting from exposure to the use environment cannot always be determined by considering each environmental stress in isolation. For instance, consider the non-linear combined effects of severe thermal and vibration stress application. A given magnitude of random vibration at elevated temperature (near or above T_g) may produce increased PWA flexure because of increased board softness or flexibility. Simultaneously, solder joint pull strength is decreased at the elevated temperature. The result may be overload, that is, a PWA configuration for either the elevated temperature or the vibration applied at room ambient temperatures may fail prematurely in service when exposed to the two factors together. Board stiffness and damping as discussed in section 4.0 are key factors to be considered. The adequacy of a proposed design may require combined-environment stress testing of prototypes prior to full-scale production. See also the references by Steinberg and Engel regarding vibration, shock and thermomechanical effects on PWA, section 9.16.

3.1.14 Insulation Resistance

The emerging advanced technologies are characterized by denser packaging resulting in ever finer conductor line widths and spacings. Without changes in the material and the operating environment, which for economic and practical reasons are not likely, finer lines and spacings result in reduced insulation resistance and increased threat of CAF (conductive anodic filament) formation. The DfR principles listed in Appendix C need to be kept in mind in the design and application of these emerging technologies.

The damage mechanisms work generally in two distinct regions: at the surface and in the bulk of the electronic assemblies, particularly the printed board. The measured insulation resistance will depend upon the nature of the laminate, solder mask and/or conformal coating under investigation. It will also depend upon the degree of cure of the polymers and for printed boards on the quality of the drilling process for the plated-through holes (PTHs) and vias (PTVs), and will be affected by soldering flux/paste

residues if they dissolve into the polymeric material during the soldering and/or cleaning processes.

3.1.15 Solvent Compatibility Surface Mount printed wiring Assemblies (PWA) are subjected to solvents (including water) and chemicals during manufacture, rework, repair and service. These agents include those used in soldering (alcohols, glycols and other solvents in flux vehicles at temperatures approaching 150°C), in cleaning the assembly after solder (saponifiers, neutralizers, hot water, terpene, mixtures, hydrochlorofluorocarbon (HCFC) mixtures and other halogenated solvents and blends at moderate process temperatures), during removal of conformal coatings with various chemicals, and during service (hydraulic and cooling fluids and fuels in military applications; alcohols and halogenated hydrocarbons during cleanup). These solvents and chemicals can adversely affect the solder mask (SM), printed wiring board, conformal coating, printed board or component legends and markings as well as degrade thin or mechanically stressed sections of plastic components. See Appendix I.

3.1.16 Corrosion The result of corrosion is material loss of the metallic conductors, permanent or intermittent continuity loss due to build up of non-conductive corrosion residues (particularly between contacts) and permanent or intermittent shorts due to build up of conductive corrosion residues and conductive metal dendrites. Corrosion accelerates the failure of components under cyclic fatigue conditions.

The oxides of tin, nickel and copper are not good conductors. Low interfacial pressure contacts to these metals can become resistive or intermittent. See Appendix L for details.

3.1.17 External Radiation External radiation typically includes X-Rays, β-particles and cosmic rays. It affects the semi-conductor material through the generation of hole-electron pairs in the bulk of the device. The purpose of understanding the radiation effects is to enable the development of radiation-hardened devices.

External radiation affects the different semiconductor devices in different ways. For instance in bipolar types, radiation causes an increase in low-frequency noise, high leakage current across the p-n junctions, and a reduction in current gain; in MOS types, a threshold voltage shift, a reduction in transconductance and an activation of parasitic elements are observed. See Appendix E.

3.1.18 Space Environment The space environment presents an unusual set of conditions which requires careful evaluation (low air pressure, low gravity, low temperature and radiation). See Appendix O.

3.2 Thermal Design The primary thermal parameter which the designer must address is the temperature of the junction or active film of the component; both the absolute maximum or peak temperature and the steady state operating temperature limits imposed by the component manufacturer (as modified by derating protocols) must be observed. The secondary thermal parameter is the solder joint temperature since long service times at high temperatures will result in grain growth in the solder, growth of the intermetallic compound layers; and large temperature swings in service will subject the joint to conditions leading to cyclic fatigue. See Appendix D for details.

Variation of the external (outside of the equipment enclosure) ambient temperature is one of the multitude of factors that will determine the actual temperature cycle a specific surface mounted device will see in operation. Very simple equipment, powered continuously at constant power will see the same temperature swings as the external ambient. In some cases, the system designer introduces built-in means of reducing the temperature swing inside the cabinet, such as fans activated when the inlet air temperature exceeds certain limits or inlet air heaters which are activated when inlet air temperature drops below certain limits.

In many applications, the variation of the temperature inside the electronic enclosure is generated by variations of the power dissipated by the electronics itself. Examples of this type of behavior are on/off periods for the systems, and fluctuations in the power dissipation as in telecommunication equipment due to variations in the number of simultaneous calls passing through the system.

It follows that different devices inside the same system might be subjected to very different temperature cycles. In order to assess the reliability of the solder joints, the designer must perform a complete thermal analysis at the device level.

In most applications, the temperature variations at a particular component in a system result from a combination of system-external and system-internal temperature variations combined with power dissipation fluctuations within the component.

3.3 Printed Board Design and Layout The printed board design and layout task, particularly for surface mount technology (SMT), has become more difficult and complex.

The difficulty of SMT designs has increased with the increase in conductor density as a result of decreases in termination pitch, conductor width and conductor spacing. The complexity of SMT designs has increased with the need to consider:

a) thermo-mechanical effects such as solder joint reliability (see section 3.4, 3.6 and Appendix A)

b) testability and inspectability (see section 8 and

Appendix J) to reduce evaluation time and cost

c) corrosion avoidance - pertinent cleaning, component clearance and conductor spacing issues (see Appendices E, L and N and section 7.5, 7.8)

d) control of electrical transients which become more severe with the increased speeds and power density of SMT designs. (See section 3.1 and Appendix E and the issues of increase in "ground bounce" and signal reflection noise.)

e) thermal design and control of the critical junction and solder joint temperatures (see section 3.2 and Appendices A, B, D and E)

f) manufacturability for high yield/quality assemblies (see section 7.8 and Appendix K) including orientation, solder thiefs

g) ESD susceptibility mitigation of components through a combination of layout and software. (See Appendix H)

h) Component placement and orientation for enhanced robustness to flexing, vibration and shock during the assembly process as well as in the use environment. (See Appendix E) The significant IPC document for this section is IPC-SM-782

i) the impact of the limited heat transfer available from solder joint to internal heat "sinks."

3.3.1 Thermal Design and Layout Where there are thermally sensitive components, heat dissipaters should generally be "downstream" in the air flow. Under certain conditions of PWA geometry, component orientation and relative component heights, turbulence may result in "recirculation cells" conveying heat "upstream."

3.3.2 Thermal Design and Conformal Coating Reduced heat extraction from the PWA (and increased junction temperatures) may result if conformal coating covers heat conduction surfaces on the PWA edge or margin which mate with heat sinks such as card-edge clamps and cold plates. (See Appendix D)

3.3.3 Land Patterns Surface land patterns define the sites where the components are to be soldered to the printed wiring board. The design of land patterns is very critical because it is the land pattern that not only determines the solder joint strength and hence the reliability of solder joints but also impacts the solder defects, cleanability, testability, and repair/rework. The very producibility or the success of the printed board is dependent upon the land pattern design.

There are certain general guidelines that one should develop to cope with the variations in tolerances of components. The selected vendor's components must pass all package qualification requirements. Standardization of parts reduces the tolerances that the land pattern design will have to support.

A second desirable requirement is that the land pattern design be transparent to the soldering process to be used in manufacturing. This will not only reduce the number of land sizes in the CAD library but it will also be less confusing for the CAD designer.

3.3.4 Balance About Neutral Axis Balanced conductor plane distribution about the neutral axis results in a SM printed board which does not "potato-chip" during the high temperature exposures and results in reduced mechanical stress on component bodies and on solder joints.

3.3.5 Vias Via holes are used to connect surface mounted component lands to conductor layers. They may also be used as test targets for bed-of-nails type probes and/or rework ports. Via holes may be tented if they are not required for node testing or rework. When a via is used as a test point it is required that the location of a test land be found to match the standard grid of the test fixture.

Buried Via A plated-through hole connected to neither the primary side nor the secondary side of a multilayer packaging and interconnecting structure; i.e., it connects only internal layers.

Blind Via A plated-through hole connected to either the primary side or the secondary side and one or more internal layers of a multilayer packaging and interconnecting structure.

IPC-TR-579 noted possible reliability problems for PTVs with small diameters and/or large printed board thicknesses. Copper plating quality in the barrel was found to be a significant parameter; nickel over plating in the barrel increases the robustness of the PTV to temperature cycling.

Use of blind and buried vias can result in effective aspect ratios (AR) much lower than the AR of PTVs in the same substrate with the same diameter. See section 3.6.

Open or untented PTVs (no solder mask on either side of the printed board) can allow liquid flux to be trapped with potential for corrosion, reducing SIR, contaminating test fixtures and causing electrochemical corrosion. (See IPC-D-275) If solder mask is intended to plug or tent these holes, it must do it consistently. Another method to prevent flux from being trapped in these vias is to plug them with solder (which wave soldering does automatically).

3.3.6 Printed Board Trace Widths and Spaces Minimum trace widths should be reviewed keeping in mind the influence of etching tolerances, undercutting, "Mousebites," and plated grain size as well as the possibility for electromigration due to current density, Joule heating and

subsequent conductor temperature rise.

Minimum trace spacings should be reviewed keeping in mind the influences of DC voltage and possible electrochemical migration, AC voltage and possible corona leakage currents, high humidity and possible electrochemical migration, low air pressure and possible corona leakage currents/premature voltage breakdown, and conductive or corrosive contamination from the ambient. See IPC-D-275, IPC-SM-782, and IPC-TR-476 and IEC 664.

3.3.7 PTH and PTV Thermal Isolation/Relief Large conductor areas such as ground planes, power planes and thermal planes "heatsink" PTH and PTVs to which they connect. During the soldering or reflow process, the reduction in local temperature can result in "cold" solder joints, bridging or icicling and may require increased time at temperature to affect a proper and reliable solder joint. Thermal relief inner lands such as those depicted in Figure 3-2 provide a measure of thermal resistance between the external soldered lands and the heatsinking plane. The results are lower required reflow temperatures, less printed board stress, and more consistent solder joints.

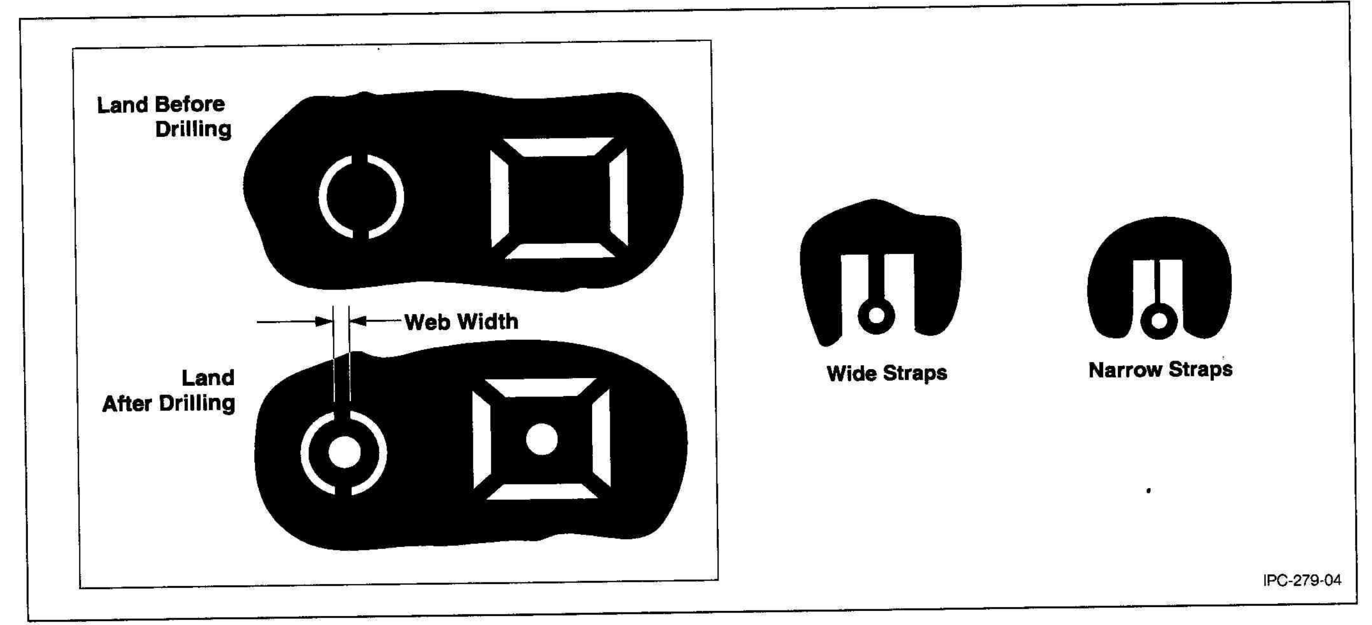


Figure 3–2 Thermal Relief in Ground Planes

3.3.8 Test Pads Test pads are required for bare-board test; see also IPC-ET-652. Previous techniques used to implement digital PWA testability such as massive addition of test nodes, become less feasible with the smaller dimensions of SMT PWAs and the number of test nodes required for components with 100-400 terminations; the mechanical force exerted by test pins is sufficient to flex and break components and solder joints.

Testability is a particular issue for field repair activities where the full capabilities of the SM PWA may not be exercised due to test equipment limitations or lack of available test time; Built-in-Test-Equipment, Built-in-Test, Built-in-Self-Test (BITE, BIT or BIST) capabilities could be invaluable in these circumstances or may be the only alternatives. See section 8 and Appendix J.

Solder mask overlap or residue on test pads (whether by design or by loss of process control) reduces test reliability. (See IPC-D-275, and IPC-SM-782)

Provide adequate margin between the land and solder mask.

Conformal coating on test pads results in diminished test accessibility; testability buss methodologies and structures may be required to permit effective and efficient fault coverage. (See IPC-SM-782)

3.3.9 Spacing Between Parts The designer should provide for manufacturability, inspectability, testability and repairability of SMT assemblies. A minimum interpackage spacing is required to satisfy all these manufacturing requirements. Some designs require that surface mount components be positioned as tightly as possible (brick-walled); these designs do not allow solder joint inspection. See figure 3-3 and section 8.0.

3.3.10 "Pads-Only" Design For this reason, many multilayer military and space applications utilize a "pads-only" outer layer design. By submerging all conductors and power planes in the inner-layers, only the land areas are exposed on the board surface. Connection to the sub-layers is then accomplished by small plated and filled vias

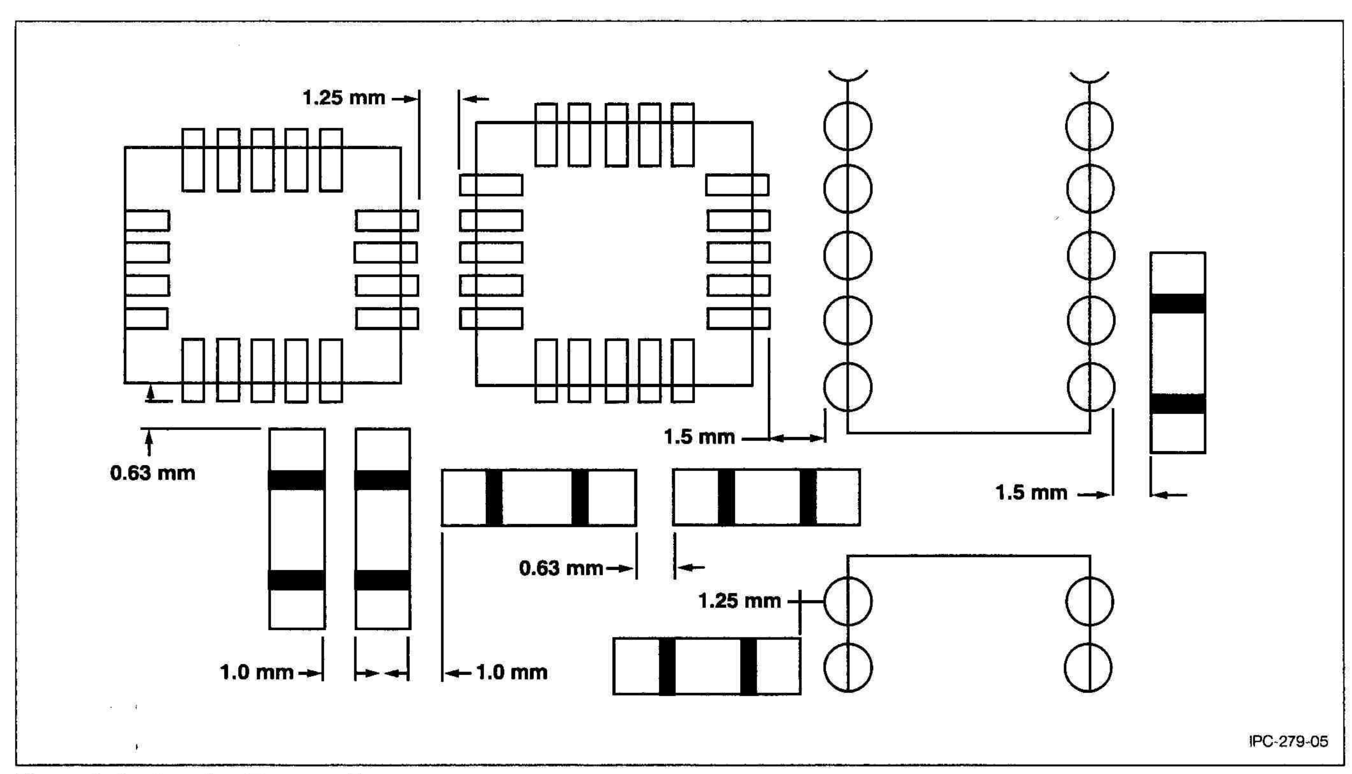


Figure 3–3 Spacing Between Parts

inside the land area. If a "pads-only" approach is not feasible, then it is crucial that solder mask be applied for surface mount designs to act as a dam to solder migration.

The "pads-only" approach has several advantages worth noting:

- the construction is compatible with soldering processes, conformal coatings and common cleaning solvents.
- The electrical and dielectric performance is no different than the remainder of the P/I structure. Stenciling of solder paste is improved.
- Application of solder mask to flexible and flex-rigid P/I structures may be difficult.
- Resolution of this approach is the same as the resolution of copper etching.

3.3.11 Components with Reduced Clearances (Traces Under) Excessively thick solder mask, particularly dry film over traces under components with small clearance, can contribute to the formation of crevices which entrap flux. In the case where the solder mask touches the bottom of the component, if insufficient solder paste is used, it may result in chip component draw-bridging (tombstoning), insufficient solder fillet or lack of solder joint. (See IPC-SM-782 and IPC-D-275.)

3.3.12 Components with Reduced Clearance and Open Vias Components with reduced clearance should not be over open vias, particularly if wave soldering is used. The vias allow flux up under the component to be entrapped in the reduced clearance space.

Heat dissipaters should generally be "upstream" of tall components to avoid recirculation cells.

Where lower junction temperature T_j is required, consider the following avenues particularly applicable to SMT: thermal vias, thermally conductive adhesives from component to printed board, and power and ground planes included in the thermal design. In addition, consider the following moves: sensitive components "upstream" of power dissipaters, power dissipaters further apart to reduce power density, power dissipaters closer to cold wall (edge of card if card clamps are used), and power dissipaters "upstream" of tall components.

Long, tall components such as connectors are ideally placed parallel to the airflow. Placement of these components perpendicular to the airflow results in the generation of recirculation cells which reduce the heat transfer from heat dissipaters or which increase heat transfer to heat sensitive components.

3.4 Coefficient of Thermal Expansion (CTE) and CTE-Mismatch Electronic assemblies consist of a multitude of elements of different materials. These materials have different coefficients of thermal expansion (CTE), of which some are listed in Appendix G. Some CTEs also vary with temperature. Because of external temperature variations and internal heat generation and different thermal resistances,

different locations within an electronic assembly are typically at different temperatures.

Matching the CTEs at a joint is no guarantee of freedom from the problem because electronic components are their own heat sources and because there is a temperature difference between component and substrate. The problem is directly related to the size of the component, the thickness of the solder joint and the compliance of the lead. The major problem arises from thermally induced cyclic stress in the solder joint of the leadless ceramic chip carrier (LLCCC) components. Some components are very easy to assemble, test and repair; others are not. The availability of a component, its performance data, its degree of testability, its reliability and its compatibility with manufacturing and assembly processes and equipment influences component selection.

3.5 Solder Joint Reliability The reliability of the surface mount solder attachment of components to the printed circuit boards depends on a number of different parameters. Some of these parameters are under the direct control of the designer, some can be influenced by the designer, and some are beyond the control of the designer.

Also, some of these parameters have a very strong influence on reliability. Relatively small changes or inaccuracies in these primary parameters have a large impact on the reliability. The impact of these parameters can be seen from the reliability prediction Equations A-3 and A-4 in Appendix A, Solder Joint Reliability.

3.5.1 Primary Design Parameters The following are design parameters that have been identified as having a primary (order of magnitude) influence on SM solder attachment fatigue reliability.

3.5.1.1 Component Size The physical size of the component determines the amount of displacement a solder joint experiences during thermal expansion/contraction of the component and the substrate to which it is soldered. Larger components are larger threats to reliability. The component size is determined by the number of I/Os and the pitch.

3.5.1.2 Attachment Type The choice of attachment type (leadless or leaded) determines the maximum stress level that can be experienced in a solder joint during thermal cycling. The stiff leadless attachments typically stress the solder beyond the yield strength, whereas compliant leaded attachments typically do not. This choice determines the reliability model that needs to be applied and affects the statistical failure distribution (Weibull slope). Leaded attachments provide larger reliability margins, which increase with decreasing lead stiffness. It needs to be noted that lead compliance can vary greatly depending on the lead geometry. Lead stiffnesses as high as 1100 N/mm for SM connector header leads and as low as 1.5 N/mm for fine-pitch S-leads have been determined.

3.5.1.3 Solder Joint Height The solder joint height determines the strain level experienced in the solder joint for a given component/substrate displacement. It results from the solder-filled gap between the component metallization or component lead and the substrate pad. Higher solder columns reduce the strains in the solder joints and increase reliability. Solder joint height is not the height of the fillet. For leaded attachments the solder joint height is not a measurable quantity; it has been defined in terms of the solder paste stencil thickness.

3.5.1.4 Solder Joint Area Solder joint area determines the stresses in a solder joint resulting from a given component/substrate displacement. It is of importance primarily for compliant leaded attachments. Larger solder joint areas reduce the applied stresses and increase reliability; however, the possible range of effective increase in area is very limited.

3.5.1.5 Lead Stiffness The lead stiffness determines the forces resulting from a given component/substrate displacement. Because the corner solder joints experience the largest displacements and the displacements are in the direction of the component center (neutral point), it is the diagonal lead stiffness which is of primary importance. Lower lead stiffness results in increased reliability.

3.5.1.6 Coefficient of Thermal Expansion The linear coefficient of thermal expansion (CTE or α) represents the change in linear dimension of a material due to a change in its temperature. Components and substrates consist typically of a variety of materials all having different CTEs; the effective CTEs are a combination of the individual material CTEs and typically are different in different directions of components and substrates. CTEs need to be measured to avoid possible large errors in the reliability predictions. See Appendix G for CTE values of different materials.

3.5.1.7 CTE - Mismatch The CTE-mismatch (ΔCTE or $\Delta\alpha$) is the difference between the coefficients of thermal expansion (CTE) of two materials or parts joined together; in most instances it is the CTE-mismatch between component and substrate, the global expansion mismatch, that is most important, while the CTE-mismatch between the solder and the materials to which it is bonded (ceramic, alloy 42, Kovar), the local expansion mismatch, plays a smaller, but not negligible role. In some designs (ceramic component on ceramic or silicone substrate), this local CTE-mismatch assumes primary importance. Large CTE mismatches pose large reliability threats; the effect of power dissipation within the component makes CTE matching not

the optimum solution (see A-2.3 and A-3.6 for explanations).

3.5.1.8 Cyclic Temperature Swing The cyclic temperature swing (ΔT) of components and substrate is the difference in the maximum and minimum steady-state temperatures experienced during either externally (daily) imposed temperature variations or operationally (on/off, load fluctuations) imposed variations. It needs to be realized that the temperature swing of the components is typically not the same as the temperature swing of the substrate due to the power dissipated in active devices. Smaller ΔTs result in improved reliability. It needs to be noted that for some applications the temperature swings during transport and storage prior to operation can be more severe and a bigger threat to reliability than the operating conditions.

3.5.1.9 Cyclic Expansion Mismatch The cyclic expansion mismatch, $\Delta(\alpha\Delta T)$ results from the difference in the thermal expansion of components and substrate which are determined by the respective thermal expansion coefficients (CTE) and cyclic temperature swings (ΔT). Smaller expansion mismatches result in improved reliability.

3.5.2 Secondary Design Parameters While the effects of secondary design parameters are, by themselves, of second-order importance, their additional contribution to the effects of the first-order parameters can be significant.

The effect of some of these second-order parameters might be different in accelerated testing and actual operational use. The effect of these secondary parameters is indirectly included in the reliability predictions of Equations A-3 and A-4 in Appendix A, Solder Joint Reliability, is the "non-ideal" factor, F. This F-factor is empirically determined.

Design parameters having second-order effects on solder joint reliability are as follows:

3.5.2.1 Solder/Base-Material CTE-Mismatch The large CTE-mismatch ($\Delta\alpha$) between the solder and some base materials (ceramic, Alloy 42, Kovar, silicon) can make substantial contributions to the cyclic fatigue damage (see A-2.3 and A-3.6).

3.5.2.2 Solder Joint Shape/Fillet/Volume Experimental evidence indicates that solder joint shape/fillet/volume have only secondary importance for reliability. In some highly accelerated tests cyclic life improvements of about a factor of two have been achieved, but it is not clear whether even these small benefits would result for the slower conditions prevalent in most product operations. The improvements result from the time necessary for crack propagation through the fillet.

Stress concentrations, e.g. from solder-mask-defined soldering lands for ball grid arrays (BGAs), can reduce the solder joint fatigue life by as much as a factor of three depending upon the severity of the loading conditions.

3.5.2.3 Solder Joint Uniformity Some experiments in which solder joints were loaded primarily in a stress-driven mode (high cyclic frequencies, no hold times, very large temperature swings with fast transitions) showed the need for extreme uniformity of all the solder joints of a component to avoid unequal stressing; accelerated tests utilizing test conditions more closely resembling product use conditions did not reveal a need for extraordinary solder joint uniformity.

3.5.2.4 Initial Solder Joint Grain Structure A fine initial grain structure in solder joints results in cyclic life improvements of about a factor of two in highly accelerated tests. The grain structure of solder is inherently unstable and will grow with time. Higher temperatures and cyclic loading accelerate the grain growth. Thus, for most product applications a fine initial grain structure will not result in a significant improvement of fatigue life; the solder joints of accelerated test vehicles should be artificially aged to start the tests with more product-related grain structures.

3.5.2.5 Conformal Coating Conformal coating can have different effects on solder joint life during thermal cycling depending on the type of material, thickness, and location. The advantage of conformal coating is that it slows the absorption of water and oxygen into surface cracks. The presence of oxides on the cracked surfaces may accelerate the crack propagation. Oxidation layers prevent "re-welding" of the solder during crack closure.

On the negative side, conformal coating may add another material with a very high thermal coefficient of expansion which may influence reliability. This addition can be significant especially if the coating wicks under components, filling the gap between the printed board and component. In addition, conformal coating can become rigid below the glass transition temperature. This condition can exert considerable stress on the components and solder joints during the thermal cycles.

Because of the large variation in conformal coating material properties, thickness applied, methods of application, etc., the effect of conformal coating, in general, needs to be evaluated empirically for each application.

3.5.2.6 Compliant Substrate Surface Layers Compliant layers at substrate surfaces can provide additional reliability margins, but by themselves are not adequate to counteract the effects of large expansion mismatches.

3.5.2.7 Solder Composition The most widely used solder compositions are eutectic (63/37) and 60/40 tin-lead solder. Solder compositions other than these can have

somewhat higher or lower fatigue reliability and are, on the whole, significantly less well characterized from a reliability point of view.

3.6 Plated-Through Hole and Via Reliability In surface mounting the plated-through holes (PTHs) have been reduced to the single function of providing electrical connections through the circuit board. Because the PTH-vias (PTVs) no longer need to be able to accept component leads, there is no need for the traditional large PTH diameters. The drive towards higher circuit board densities also has put pressure on designers to reduce PTV diameters. At the same time, the number of layers and, thus, the circuit board thicknesses have been increasing. Therefore, the PTV aspect ratio (the ratio of circuit board thickness and drilled PTV diameter) has been increasing. The results of an IPC round robin study (IPC-TR-579, Round Robin Reliability Evaluation of Small Diameter Plated Through Holes in PWBs) show that for PTVs with aspect ratios (AR) > 3, special care is necessary to produce high quality PTVs. Copper plating quality in the barrel was found to be a significant parameter; nickel plating in the barrel increases the robustness of the PTV to temperature cycling.

The PTVs are most stressed during temperature excursions into the solder reflow range. For high quality PTVs five (5) excursions to solder reflow temperatures consume about 1/6 of the available fatigue life of the PTH-via copper barrels; for low quality PTH-vias the solder reflow operations can cause PTH-via barrel fracture during manufacture. For high quality PTH-vias the 1/6 loss of available life is not significant; however, for applications with more severe use conditions (see Table 3-1) this 1/6 loss of life could be a sizeable portion of the design life.

The most important aspect of high quality PTVs is the quality of the copper deposit in the via barrels. As the PTV's aspect ratio increases, it becomes more difficult to plate high quality, uniform copper deposits inside the holes. Special electrolytic plating formulations or electroless plating may be required.

3.7 DfR of SM Solder Attachments The material in Appendix A gives a detailed treatment of DfR of solder attachments.

3.8 DfR of Insulation Resistance The material in Appendix C gives a detailed treatment of DfR with regard to Insulation Resistance.

4.0 SUBSTRATES

This section addresses the materials related issues of substrates. For printed board design and layout, see section 3.3 above.

See also IPC-D-275 for more details on rigid boards.

4.1 General Substrate Categories Interconnect substrate technologies can be divided into the following categories:

1. Organic based printed wiring board
2. Discrete wiring printed board
3. Ceramic based printed circuit board (thick film, co-fired)
4. Ceramic based printed circuit board (thin film)

Categories 1-3 above can be further classified:

Type 1—Single sided

Type 2—Double sided

Type 3—Multilayer with blind or buried vias

Type 4—Multilayer with blind and/or buried vias

Type 5—Multilayer metal-core board without blind or buried vias

Type 6—Multilayer metal-core with blind and/or buried vias

Type 7—Rigid-flex multilayer without blind or buried vias (organic only)

Type 8—Rigid-flex multilayer with blind and/or buried vias (organic only)

See Table 4-1 for the advantages and disadvantages of common substrates.

Surface mount components are held on these substrates with solder. The components normally have a different CTE than the substrate; consequently, there will be mechanical stresses on solder joints as the ambient temperature changes. The cycling stress is a potential reliability problem. To minimize this problem, packages can use compliant leads and have the CTE matched to that of the substrate. Substrates are also used for removal of heat. Selected substrates must maintain their function in adverse environmental conditions and be manufactured/assembled at reasonable cost.

Substrates for surface mount technologies include the most commonly used fiber glass reinforced epoxy system with flame retardant, FR-4. The next commonly used material is polyimide glass because of its higher temperature. Each of the materials has its own particular characteristics and properties and behaves differently under varying conditions of temperature, humidity, and other stresses.

4.2 Substrates and Their Functions:

a. Power distribution;

b. Signal distribution, interconnecting lands to each other and to the next level with acceptable signal integrity;

c. Structural, providing a stable platform with a CTE close enough to that of the components that sufficient reliability under use conditions is obtained.

For the assembly to function properly, the electrical, mechanical, and thermal requirements of each material used in the substrate must be considered for the operating conditions and use environments.

Table 4-1 provides guidance in the material choices. See IPC-D-275 for other material discussions.

4.3 Moisture and its Effects on Polymer Substrates Polymers commonly used in SMT printed boards absorb and adsorb water when exposed to moist atmospheres (high relative humidity) for durations ranging from several days to several weeks; the equilibration time depends upon the thickness of the laminates and the geometry of the conductor pattern. The relative permittivity of water is 80 and that of common substrates ranges from 3 to 5; the absorption of 1-3% by weight of water can significantly (but reversibly) increase the dielectric constant between conductors and hence the capacitive coupling between conductors, over time. The absorption and adsorption of water also decreases the insulation resistance between conductors at the surface (SIR). Together with ionizable contaminants and DC bias, condensed moisture can lead to electrochemical corrosion and dendrites on the surface of the substrates; conductive anodic filament (CAF) formation at the glass fiber-resin interface; and electrochemical corrosion and dendrites at delaminations and voids such as occur between conductors on inner layers and between barrels of PTVs and PTHs. Moisture effects are more significant in SM printed boards because the spaces between conductors and the interbarrel distances are much less than the corresponding dimensions in through hole printed boards; in addition, solder masks may not be easily applied between land patterns in the fine and extra fine pitch SM patterns. See Appendix C for DfR information on SIR. See also IPC-TR-476.

Some materials with higher glass transition temperatures (T_g) such as bismaleimides and polyimides, appear to absorb more water than the lower T_g materials, such as the epoxies. Drying of the higher T_g materials (as well as thicker buildups of the epoxy systems) prior to SM reflow exposure or rework/repair is recommended to minimize delamination or separation, for instance, of the conductor from the resin or the glass fiber from the resin.

The laminate surface is porous when treated by etching to enhance adhesion of conductors; this surface porosity can retain hydrolyzable and ionizable contaminants and water, as well as hydrophilic materials such as polyglycols which are used in the formulation of some water soluble SM solder pastes. Solder mask and conformal coating materials cover and seal the porous surface and help to retain SIR values and reduce the risk of corrosion.

Common solder masks (and conformal coatings) are permeable to water vapor; the presence of water soluble contaminants between solder mask or conformal coating and the underlying surface can result in vesication or mealing and in electrochemical corrosion/migration.

Chemisorption of water into polymers appears to reduce the T_g slightly, reduces the adhesion of the polymer to other materials and reduces the strength of the polymer. See also the bibliography of IPC-SM-786.

4.4 Coefficient of Thermal Expansion (CTE) of Polymer Systems Polymer systems expand with increasing temperature, demonstrating a glassy phase response below T_g with a CTE or α_1 and a rubbery phase response above T_g with a much higher α_2, typically 3 times α_1. The transition from glassy phase to rubbery phase is gradual, but for most polymer substrates may be characterized by T_g, the glass transition temperature.

Glass fiber reinforced substrates exhibit significantly different CTE in the z (out of plane) axis compared to the CTE in the x and y axes; for example, below its T_g, Quartz/Bismaleimide material with 35% resin by weight exhibits a CTE(x-y) of 6 ppm/°C and a CTE(z) of 41. Woven glass fiber reinforcement exhibits an additional difference between x and y axes on the order of 1-5 ppm/°C; this difference may be significant where the CTE of a large SM component package is to be matched to the CTE of the substrate to enhance cyclic life of the solder attachments.

The CTE(z) is particularly significant in determining the cyclic life of PTH and PTVs in SM PWAs because the aspect ratio (ratio of substrate thickness to finished hole diameter) is generally much larger than the corresponding aspect ratio achieved in printed boards manufactured for through hole technologies. Higher CTE(z) values result in higher cyclic tensile stress in the barrel of the PTH or PTV during temperature excursion during SM reflow, or SM component removal/rework/repair as well as during printed board fabrication, solder dipping, hot air leveling, or wave solder. See IPC-TR-579 and IPC-SM-782.

The thermal cycle reliability, vibration robustness, and the thermal management of high performance Surface Mount (SM) products are heavily dependent upon the constraining core such as copper-molybdenum-copper (CMC), copper-Invar-copper (CIC) and molybdenum-graphite-molybdenum (MGM) composite material systems.

The ratios of the various materials in those composite systems can be adjusted to tailor the effective CTE to the optimum value. The tradeoffs include weight and cost. See IPC-MC-324.

4.5 Constraining Cores in Substrates A constraining core is an internal supporting plane in a packaging and interconnecting structure, used to alter the coefficient of thermal expansion of printed boards.

Table 4–1 Advantages and Disadvantages of Various Types of Substrates

TYPE	MAJOR ADVANTAGES	MAJOR DISADVANTAGES	COMMENTS
ORGANIC BASE SUBSTRATE			
Epoxy fiberglass	Substrate size, weight; reworkable; dielectric properties; conventional board processing, availability, cost/performance value.	Thermal conductivity	x, y, and z axis CTE a concern for high density applications.
Polyimide fiberglass	Same as epoxy fiberglass plus high temperature z axis CTE; substrate size; weight; reworkable, dielectric properties.	Thermal conductivity; moisture absorption.	Same as epoxy fiberglass; x, y, and z axis CTE a concern for high density applications.
Epoxy aramid fiber	Same as epoxy fiberglass; x-y axis CTE; substrate size; lightest weight; reworkable; dieletric properties.	Thermal conductivity; resin microcracking; z axis CTE; water absorption; cost; resin adherence.	Volume fraction of fiber can be controlled to tailor x-y CTE. Resin selection critical to reducing resin microcracks.
Polyimide aramid fiber	Same as epoxy aramid fiber; z axis CTE; substrate size; weight; reworkable; dielecric properties.	Thermal conductivity; resin microcracking; water absorption; cost; resin adherence.	Same as epoxy aramid fiber.
Polyimide quartz (fused silica)	Same as polyimide aramid fiber; x, y, z axis CTE; substrate size; weight; reworkable; dielectric properties.	Thermal conductivity; drilling; availability; cost; low resin content required.	Volume fraction of fiber can be controlled to tailor x-y CTE. Drill wearout higher than with fiberglass.
Fiberglass/Teflon laminates	Dielectric constant; high temperature stability; thermal conductivity; x and y axis CTE.	Same as epoxy fiberglass; low temperature stability; thermal conductivity; x and y axis CTE; difficult processing.	Suitable for high speed logic and high frequency applications. Same as epoxy fiberglass.
Flexible dielectric	Lightweight; minimal concert to CTE; configuration flexibility.	Size	Rigid-flexible boards offer tradeoff compromises.
Thermoplastic	3-D configurations; low high-volume cost.	High injection molding setup costs; additive processing.	Very limited applications.
Bismaleimide/triazine glass	Improved dielectric properties; multiple thermal shock; minimum cost penalty for upgrade.	Thermal conductivity; x, y, and z axis CTE.	Applicable to MCM-L technology.
Composite CEM-1 and CEM-3	Punchable at room temperature; cost; stiff enough for SMD.	x and y axis CTE; thermal conductivity.	Substrate of choice for consumer products with SMDs.
Paper-based phenolic	Punchable with heat; lowest cost.	Single-sided only; stiffness; availability; x and y axis CTE.	Majority of world market is paper-based.
NONORGANIC BASE			
Alumina (ceramic)	CTE; thermal conductivity; conventional thick film or thin film processing; integrated resistors.	Substrate size; rework limitations; weight; constant; brittle; dielectric constant.	Most widely used for hybrid circuit technology.
SUPPORTING PLANE			
Printed board bonded to plane support (metal or nonmetal)	Substrate size; reworkability; dielectric properties; conventional board processing x-y axis CTE; stiffness; shielding; cooling.	Weight	The thickness/CTE of the metal core can be varied along with the board thickness, to tailor the overall CTE of the composite.
Sequential processed board with supporting plane core	Same as board bonded to supporting plane.	Weight	Same as board bonded to supporting plane.
Discrete wire	High speed interconnections; good thermal and electrical features.	Licensed process; requires special equipment; cost; availability.	Same as board bonded to low expansion metal support plane.
CONSTRAINING CORE			
Printed board bonded with constraining metal core	x and y axis CTE; uses FR-4 or polyimide/glass materials.	Weight; internal layer registration; delamination; via hole cracking, z axis CTE.	Can be used as power/ground planes.
Printed board bonded to low expansion graphite fiber core	Same as board bonded to low expansion metal cores; stiffness, thermal conductivity; low weight.	Cost; microcracking; z axis CTE.	The thickness of the graphite and board can be varied to tailor the overall CTE of the composite.
Compliant layer structures	Substrate size; dielectric properties; x-y axis CTE.	z axis CTE; thermal conductivity.	Compliant layer absorbs difference in CTE between ceramic package and substrate.

As with printed boards with supporting planes, one or more supporting metallic or non-metallic planes can serve as a stiffener, heatsink, and/or CTE constraint in constraining core printed boards.

The results of "accelerated" life tests which incorporate temperatures which approach or exceed the T_g of the substrate should not be extrapolated to predict service life; these tests may be used to discriminate between alternatives.

4.5.1 Printed Board Stiffness and Damping Constrained core systems with skins of high modulus material form boards which in comparison with standard base materials are stiffer and have higher damping frequencies. These characteristics may be beneficial, depending upon the environmental vibration and noise spectrum.

4.6 Flexible Printed Board with Metal Support Plane Another arrangement for a printed board with leadless components involves conventional fine-line polyimide flexible printed wiring. These assemblies can be constructed in multilayer form while retaining the low-modulus feature that reduces residual strain at the solder joints. Furthermore, lasers can drill very fine holes in the thin, printed wiring laminate. These holes can be plated-through or filled with solid copper as required.

To retain inherent flexibility while dissipating heat from the solder joint, cutouts in the flexible circuit accommodate pillars from the metal heatsink support plane. Although this appears to be heavy and cumbersome, if the heatsink baseplates are made from thin sheets of aluminum, the resulting density of the combined circuit/heatsink assembly might actually be less than other constructions.

4.7 Discrete Wire Structures with Metal Support Plane Discrete wire printed boards have been developed specifically for use with surface mounted components. These structures are usually built with a low-expansion metal support plane that also offers good heat dissipation. The interconnections are made by discrete 0.06 mm diameter insulated copper wires precisely placed on a 0.03 mm grid by numerically-controlled machines. This geometry results in a low-profile interconnection pattern with excellent high-speed electrical characteristics and a density normally associated with thick film technology.

The wiring is encapsulated in a compliant resin to absorb local stresses and dampen vibration. Electrical access to the conductors is by 0.25 mm diameter copper vias. The small via size can be accommodated in the component attachment land, thus eliminating the need for fanout patterns when using components with terminals on centers as close as 0.6 mm, and allowing very-high packaging densities.

The high level of water absorbed into polyimide tape automated bonding (TAB) substrate materials during exposure to high ambient moisture levels has been observed to result in conductor corrosion and delamination.

4.8 Outgassing of Polymer Substrates See also the discussion of solder mask and coatings in Appendix N, and section 6. The printed board may contribute emissions of cleaning solvent, polyglycols, and lighter fractions of flux vehicles in addition to the emission from the solder mask and conformal coating of the printed board and of the component encapsulation materials.

4.9 Assembly Process Effects on Polymer Substrates See also the discussion of rework and repair in section 7.6 and Appendix E.

In addition, fluxes for wave soldering and for water soluble solder pastes can contain high boiling point hydrophilic or hygroscopic solvents such as the polyglycols. These solvents can penetrate the resin-glass fiber interface and contribute to conductive anodic filament (CAF) formation. See Appendix C for DfR information. See also IPC-TR-476.

4.10 Printed Board Solderability The land patterns in IPC-SM-782, particularly for those intended for fine pitch and extra fine pitch components, clearly demonstrate the very small areas available for affecting the solder joint in SM technology. A solderability defect with an area of 125 µm by 250 µm which might be discounted on a through hole board may constitute the single land which is non-solderable on a SM board and render that SM PWA non-functional; worse, the component lead may contact the land and mechanically affect an electrical contact which becomes intermittent in service and the product is a NTF or No Trouble Found at the repair center.

Although solder dipping and hot air solder leveling (HASL) are said to constitute "proof" that the land is solderable, these processes do not characterize solderability of the land at the critical time which is just before the solder paste is applied and the components are placed. Printed board land solderability is degraded by oxides or chlorides of tin and lead oxides or chlorides of tin-lead phases; oxides of tin-copper intermetallic compounds; and organic films such as residues from fluxing oils, finger prints or solder mask. These oxides, chlorides and organic films can form after the HASL process. See also IPC-PE-740 and IPC-S-816. Quantification of the solderability of the SM printed board is difficult but is addressed in ANSI/J-STD-003; an earlier specification is IPC-S-805.

4.11 Design for Reliability of Plated-Through-Hole Vias (PTVs) The material in Appendix B gives a detailed treatment of DfR for PTVs.

5.0 GENERAL COMPONENT SELECTION CONSIDERATIONS

1. During circuit design and verification, primary impact on manufacturing and reliability lies in the

selection of components.

2. Commonly used components are available with information detail that simplifies layout, assembly, test, and repair. The data includes termination material and finish, termination configuration, land pattern, package construction, etc.
3. Some components are very easy to assemble, test, and repair; others are not. The availability of a component, its performance data, its degree of testability, its reliability and its compatibility with manufacturing and assembly process and equipment influences component selection.

It is important that the electronic circuit designer and the designer of the SM PWA understand that the selection and application of components cannot be isolated from selection and process flow design of the assembly processes, including inspection, test, rework, repair, and service. The surface mount reflow and wave solder processes subject the component to process stresses at levels not achieved in through-hole solder processes. These stresses and especially the components' response to reflow or wave temperatures in excess of 220°C are not normally considered in through-hole component design. Shock and vibration stresses applied to the SM PWA during depaneling can greatly exceed the stresses anticipated in service or transportation. Application-specific ICs (ASIC) and other IC components require thorough testing and test coverage prior to assembly; if the SM PWA is defective at board test, sufficient test pads must be present for effective fault location and component replacement to be made.

5.1 Component Selection Strategy The best strategy is to use parts that meet (as a minimum) JEDEC/EIA footprints and which have been qualified for the process flow including rework/repair. The characterization/qualification process should be conducted with the components mounted on coupons to simulate the process and thermomechanical stresses. These requirements apply to assembly subcontractors, as well as in-house assembly operations. See also IPC-R-700.

Component suppliers may be able to provide data on the reliability of components upon exposure to various accelerated stress conditions after exposure to various simulated reflow processes.

5.2 Package Leadframe and Local Materials Leadframe and lead materials with low CTEs, e.g. Alloy42, Kovar, etc., should be avoided for plastic surface mount components (PSMCs). Such materials lower the composite CTE of components creating large CTE-mismatches with FR-4 or similar printed board materials. Solderability problems have also been encountered with these lead materials. See also Appendix A.

5.3 Package Lead Configuration Selection

1. Surface mount devices (SMDs) are functionally not different from their conventional through-hole counterparts. What is different in surface mounting is the packaging of devices. SMDs provide greater packing density because of their small size. SMDs are available in numerous package types and lead configurations (see IPC-D-275 and IPC-SM-782). For further details on specific components, reference Appendix F.
2. In the selection of SMDs, consider such differentiating factors as termination configuration, availability, and real estate consideration. For complex function SMDs, testability is an additional factor; see Section 8.2 and Appendix J on DfT.

5.3.1 Gull Wing Components The gull-wing leads of small outline integrated circuit (SOIC) packages are easier to inspect than the J-leads on plastic leaded chip carriers (PLCC). Gull-wing leads can be soldered using various processes, are more uniform (simplifying routing) and more accessible for testing purposes (but must not be directly contacted with probe pins to avoid damage at the lead-package interface). The disadvantage is that gull-wing leads protrude from the package (occupying valuable board space), and particularly on packages without corner bumpers, are susceptible to damage during shipping and handling.

5.3.2 J-Lead Components J-leads are more space efficient than gull-wing leads and can also be soldered using most reflow processes. J-leads are sturdier and more resistant to shipping and handling damage. The compactness of J-leaded components, however, can complicate routing and reduce test access. However, some J-leads have higher lead stiffness increasing the fatigue damage to solder joints.

5.3.3 Pin Grid Arrays Pin-grid arrays (PGAs) require more real estate and board layers, especially if a fine line fabrication is not being used. Some PGAs have hundreds of pins that occupy large sections of every routing layer with complex break out patterns.

5.3.4 Fine Pitch Components The potential complications of the fine pitch SMD are balanced by its smaller footprint. Fine pitch SMDs are more difficult to rework, service, and test; they are also more difficult for assembly equipment to handle than standard SMDs. Because fine pitch terminations and tolerances are much smaller, they may require a robotic arm as opposed to pick and place equipment for accurate placement. In many situations, there are no packaging alternatives because some devices are so complex that only one or two package types are available.

5.3.5 Plastic Surface Mount Components (PSMC) PSMCs, including semiconductors and resistor/capacitor networks, should have measured data on maximum body temperature (Tmax) for the process flow, including rework/ repair. PSMCs should be obtained from suppliers who have control of moulding voids, internal and external package cracks at the bonding fingers, and qualification or characterization of the PSMCs to the peak process temperature while meeting the requirements of IPC-TM-650, Method 2.6.20 (see Appendix F).

Surface mounted plastic ICs absorb moisture from atmosphere humidity by diffusion. During assembly reflow processes, rapid moisture expansion and material mismatches can result in cracking and/or delamination of critical interfaces within the packages. The classification levels defined in IPC-SM-786, Standard for Handling and Shipping of Moisture/Reflow Sensitive ICs, are intended to be used by IC producers and IC users (board assembly operations). The levels of moisture sensitivity of product devised should be used to avoid package cracking and delamination.

Susceptible components should be required to be dried (baked) and bagged by the supplier and subject to appropriate documented internal or subcontractor treatment during production and rework/repair; these treatments limit additional internal delamination and cracking, but do not reverse existing delamination and cracking.

See Appendix F and IPC-SM-786 for more details on PSMC performance under SM solder reflow conditions. See Appendix E for additional detail on rework and repair effects on PSMCs.

5.3.6 Component Termination Coplanarity and Configuration A critical issue in SMDs is lead coplanarity which is defined as lying or acting in the same plane. Non-coplanarity is the distance between the lowest and the highest leads when the package rests on a perfectly flat surface. The common problem caused by non-coplanarity is the phenomenon known as solder wicking (the solder paste wicks up the lead, causing open solder joints). It should be kept in mind that poor land or lead solderability or uneven or fast heat application during the reflow process also can cause open solder joints. For all these reasons, the lead ends should lie perfectly in the same plane to avoid manufacturing problems.

5.3.7 Component Lead Configuration Each lead configuration has its advantages and disadvantages. Butt-lead or I-lead devices are not commonly used. The advantage claimed for butt-leads is the possibility of converting through-hole components into SM by clipping the leads and accomplishing the soldering of all components in one reflow operation. Butt-lead joints have normally 65% less pull and shear strength than joints to J or gull-wing terminations and are more sensitive to process-related handling, placement and reflow soldering, and are less compliant than J-leads or gull-wing joints.

5.4 Component Termination Finishes Ceramic and ferrite components such as multilayer ceramic capacitors, chip resistors, and chip inductors are generally terminated with a fired-on silver or silver palladium paste. Because the silver content is easily and rapidly dissolved or leached into molten solder, the soldering process window is tightly constrained as to temperature range and peak temperature duration. A high silver content in the solder joint results in loss of ductility. A termination with high loss of silver is weakly adherent to the ceramic (see 5.4.1).

5.4.1 Nickel Barrier Layer An overplating of nickel (which dissolves at 1/10th the rate of silver) is recommended as a barrier layer between the silver bearing paste and molten solder. Nickel oxide and nickel corrosion compounds are resistive and difficult to solder; nickel oxidizes or passivates rapidly. To prevent oxidation and corrosion of the nickel and hence to preserve the solderability of the termination, an easily soldered final metallic termination finish such as tin, tin-lead or gold is used; palladium is used on some compliant leads.

5.4.2 Tin and Tin-Lead Solder Termination Finishes The most common SM component termination finishes include tin and tin-lead. Tin-lead finishes are also called solder finishes. Because copper diffuses into the tin-lead and forms copper-tin intermetallic compounds (Cu_3Sn or Cu_6Sn_5) at elevated temperatures, an ideal metallurgical system for copper terminations includes a barrier layer of nickel. The formation of the intermetallic compounds results in a lead rich layer on the termination. The oxides and chlorides of lead, copper-tin IMCs, Cu_3Sn, and Cu_6Sn_5 and the chlorides of tin often are difficult to solder.

5.4.2.1 Tin-Only Finishes Tin-only finishes may exhibit tin "whiskers" as a result of stresses in the tin or nickel under-layers; the whiskers may short closely spaced conductors. Tin-only finishes may also exhibit stress induced in tin "pest," an allotropic transformation of the white tin to a friable grey tin at low temperatures (~–40°C) alloys with lead, bismuth, or antimony are less susceptible. Lead content > 3% appears to suppress both whiskers and pest; alloying of the tin with the lead in tin-lead solder pastes or molten wave solder appears to be sufficient to prevent the emergence of either problem according to extensive stress tests conducted on tin-terminated multilayer ceramic capacitors.

Pure tin plating is not recommended.

5.4.2.2 Tin-Lead Finishes Tin-lead finishes can be applied by electroplating or by dipping of the termination into molten solder. Plated (but non-reflowed) finishes are

uniform in thickness. Plating may be followed by a reflow performed in hot oil. Dipped or reflowed solder finishes are thinner at the corners of the terminations. Dipped solder finish processes are sometimes followed by hot air "kniving" to obtain a uniform thickness of metal on the flat portion of the termination; the result is the thinner metal at the corners. Copper terminations are commonly less solderable at the corners due to exposed intermetallics and oxidation of the intermetallics more quickly than areas with thicker tin-lead coating.

5.4.3 Termination Recommendations When Using Electrically Conductive Adhesives Where electrically conductive adhesive is used, component termination finishes of silver, gold or palladium are recommended, since silver oxide is conductive and gold and palladium do not oxidize. Tin, lead, or tin-lead terminations are not recommended, particularly when the service environment exposes the joints to humidity. The moisture permeates the adhesive and oxidizes the adhesive/metal interface, increasing the series resistance.

5.4.4 Gold, Palladium, Silver Termination Finishes Where gold or palladium plating is used, the gold or palladium content in the solder joint should be less than 3 wt%. This level can generally be met if the gold or palladium finish is ~0.1 µm thick on both the component termination and the printed board. Alternatively, the component terminations can be dipped in solder to remove the gold; the solder bath must be monitored to prevent excessive gold buildup. The presence of gold plating on the printed board might be driven by the use of pressure contacts such as solder-less or edge connectors.

Copper leads should be separated from gold overplating by a pore-free barrier of nickel plating to prevent diffusion of the copper into the gold; oxidation of diffused copper degrades the solderability of the gold finish.

Where thin, uniform, solderable platings are needed which can be exposed to high temperatures without loss of solderability, precious metal platings are chosen. Silver, palladium and gold are some of the precious metals available. Gold is the best of these materials having excellent solderability and the best shelf life (indefinite). However, it is expensive and prone to intermetallic failure. Gold requires a barrier layer of nickel plating, ~1.5 µm thick, to prevent diffusion of copper to the surface of the gold which degrades solderability.

Gold plating requires a careful soldering process to avoid formation of intermetallic phases which may embrittle the solder joint and lead to premature failure. Surface mounted solder joints are more susceptible to embrittlement failure because of the limited amount of solder in the joint and the reliance on the solder joint for mechanical strength. The concentration of the gold in the tinning bath needs to be monitored to prevent the gold concentration from exceeding 3 wt%.

Silver requires care in handling and storage to avoid tarnishing which can interfere with solderability.

5.5 Solderability of Termination Finishes Solderability describes an observed condition which results from the use of a flux together with a component termination finish or printed board land pattern finish under the influence of a heat source.

The period of time over which tin-lead finishes demonstrate acceptable solderability depends upon the plating thickness, plating conditions and storage conditions; solderability decreases with increases in such factors as temperature, humidity and oxygen content. Benign atmospheres and proper storage conditions may result in a shelf-life on the order of years. Some plated systems are unsolderable after several months under factory floor conditions. Techniques for evaluating and quantifying solderability are found in J-STD-002, Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires. Organic contamination such as oil, grease, and finger prints or particulate contamination such as dust can also degrade solderability. The mild no-clean or "leave-on" fluxes may not be effective in the presence of these contaminants.

Co-deposited organic materials (electroplating brighteners and levelers) will shorten the solderable shelf life of the tin or tin-lead plating.

Tarnished finishes may be difficult to solder and result from the reaction of a silver termination finish with sulfur compounds which may be emitted by chemical processes using sulfur or storage containers made from paper containing residual sulfur compounds. Silver-plated terminations should be stored with an oxidation inhibitor.

Assure solderability through testing by the producer. The wetting balance method permits measurement of the time-for-wetting as well as the degree of wetting. This testing provides a reproducible method of evaluating process variables with a standard sample geometry. At this time, interpretation of the results varies. A cheaper, non-quantitative test is visual examination of the solder tinned surface ("dip and look").

5.6 Soldering Considerations SMDs must withstand the higher solder process temperatures and must be selected, placed and soldered more carefully to achieve acceptable manufacturing yield. See also Appendix D, Components and PSMCs.

5.7 CTE Mismatch Considerations Difference in the coefficient of thermal expansion (CTE) of the materials of an SMD is very important to its reliability. This is because

at one temperature, there may be no stress where two materials join but at a different temperature, if there is a difference in CTEs, the same joint may well be under such considerable strain that the part fractures.

Matching the CTEs at a joint is no guarantee of freedom from the problem because electronic components are their own heat sources and because there is a temperature difference between component and substrate. The problem is directly related to the size of the component, the thickness of a solder joint and the compliance of the lead. See Section 3.4 and Appendix A. The major problem arises from thermally induced cyclic stress in the solder joint of the larger leadless ceramic chip carrier (LLCCC) components.

5.8 ESD Packaging Requirements All SM pick-and-place feeder parts, sensitive or not, if they are dispensed adjacent to ElectroStatic Discharge Susceptible (ESDS) components, should be packaged in antistatic materials.

5.9 Specials or Custom Devices Use Precaution Devices with unusual or exotic characteristics, extremely tight specifications, or low volume "custom" processing are not as reliable as "standards." The tightened specifications result in a smaller or unknown C_{pk}. The unique process of evaluation and selection used to meet special requirements is more vulnerable to errors. It is very difficult to demonstrate product quality and reliability (or to improve the process) with low volume of product.

5.10 Components to Avoid or to Use with Caution

- Printed board with $T_g < 125°C$
- Printed board with PTH and PTVs aspect ratio > 3:1
- Components not on the preferred parts list
- Components using obsolete technologies
- Components containing liquid and sealed only with rubber
- Components with rotating seals
- Components with thick silver or gold plating or paste as the solderable termination
- Components with corrosive or polar liquids
- Aluminum electrolytics with silver anode (obsolete technology)
- Components with exposed moving electrical contacts
- Electro-Mechanical connections between contact finishes of tin and gold (dissimilar metals)
- Film resistors trimmed more than 50%
- Multilayer ceramic components such as capacitors, inductors, filter networks assembled into PWAs using assembly processes with $\Delta T/\Delta t > 4°C$/second.
- Solder immersion or wave soldering of surface mount components other than simple chip resistors and chip capacitors.
- Components with ESD susceptibility
- Variable resistors, particularly wire-wound
- Variable capacitors
- Multilayer capacitors trimmed to value

5.11 Component Selection Considerations for Military and Space Applications Military and aerospace applications exposed to severe environments may require packages that are more robust. Hermetic packages may be required to be robust to a life cycle environment which includes high relative humidity. However, under extreme levels of shock and vibration, hermetic packages (with flying internal leads) are less robust than plastic encapsulated packages. See Appendix P.

6.0 SOLDER MASK AND CONFORMAL COATING CONSIDERATION

Because of the fine lines and close conductor spacing and the assembly processes utilized in SMT, solder mask and conformal coatings may be a new design requirement. Solder mask performs two functions, one to limit the flow of solder paste, the other to protect adjacent traces from corrosion. Conformal coating protects the solder joints and component conductors from corrosion. Detailed descriptions of solder masks and conformal coatings may be found in Appendix N.

6.1 Solder Mask Considerations for SM The decision to use solder mask for surface mount technology applications is usually based upon the need to prevent migration of solder away from the device pads during solder reflow. An alternative to the use of solder mask is a pads-only approach.

Typically, solder mask openings are designed 125 μm larger than the component land or through-hole pad. This allows for alignment tolerances during solder mask processing. Since solder mask or its residue on surface mount pads will reduce the size of the solder fillet, it is highly recommended that printed boards be procured which exclude solder mask from extending onto these areas.

The "do's" and "don'ts" of solder mask are important elements in the construction of a reliable surface mount assembly. The type, thickness, coverage areas and proper application are essential parameters in this complex equation. Since surface mount design begins to encroach upon the limits of the solder mask process, it is important for the designer to understand solder mask process capabilities. The solder mask must be compatible with the surface mount processes being used, especially the heat and solvent resistance characteristics. The choice of a particular solder mask should be validated with the proposed assembly processes (reflow, wave and rework soldering; cleaning, conformal coating) to ensure that there are no adverse

interactions. Failure to understand the links between board manufacture, assembly processes and circuit design may result in a choice of solder mask which will be costly to reverse after introduction.

6.1.1 Solder Mask Selection Table 6-1 provides guidelines on solder mask selection.

der mask and tapes are used to prevent solder and solvents from causing problems during assembly processes. In SMT the reflow techniques may expose the mask or tape to temperatures which may cause thermal breakdown. This may cause reversion of some materials into a sticky "goo" and others may adhere tenaciously making them difficult to remove. The cleaning of SM assemblies may also be more aggressive than through-hole. It is necessary to verify that the temporary mask selected is compatible with the assembly processes.

Table 6-1 Solder Mask Guidelines

			RECOMMENDED FOR THESE SM SOLDERING PROCESSES			
SOLDER MASK TYPE	APPLICATION METHOD	THICKNESS	TENTED VIAS	STANDARD PITCH REFLOW	FINE PITCH REFLOW	WAVE SOLDER
Liquid	Screenprint	8-50 µm	N*	N	N	N
Dry Film	Hot roll Lamination	60-100 µm	Y	Y	N	Y
Liquid Photoimageable	Open Screen Coat Curtain Coat Roller Coat Electrostatic Spray	15-30 µm	N	Y	Y	Y
Combination (liquid photoimageable* dry film cap layer)	Lamination	50-75 µm	Y	N	Y	

*The majority of via holes can be filled by this process but not tented.

6.1.2 Solder Mask Thickness Issues Regardless of the type of solder mask used for surface mount applications, the solder mask must be the correct thickness and consistent. Solder mask plays an important role in forming a gasket between the solder paste stencil and the printed board to reduce the extrusion of paste and limiting smearing. Typical dry film solder masks range from 75 to 100 µm thick, leaving the mask higher than the surface mount pads (see Figure 6-1). Thus, the stencil will rest on the solder mask and leave a gap between the stencil and the pads through which solder paste can flow. However, typical liquid photoimageable masks range from 15 to 30 µm thick. This makes the pad surfaces the highest points on the board so that when the stencil is lowered, it will rest on the pads. The stencil then gaskets the opening around the pads, preventing the solder paste from getting under the stencil.

Excessively thick solder mask, particularly dry film over traces under components with small clearance, can contribute to the formation of crevices which entrap flux. In the case where the solder mask touches the bottom of the component, if insufficient solder paste is used, it may result in chip component drawbridging (tombstoning), insufficient solder fillet or lack of solder joint. (See IPC-SM-782 and IPC-D-275)

Solder joint reliability under temperature cycling or power cycling conditions may be reduced if the solder mask touches the bottom of the component or conformal coating filling the printed board-component gap. (See IPC-SM-785.)

6.2 Temporary Solder Mask and Tapes Temporary solder mask and tapes are used to prevent solder and solvents from causing problems during assembly processes.

6.3 Conformal Coatings The primary purpose of conformal coatings is to provide environmental protection. Some conformal coatings have been shown to significantly affect the reliability of surface mount solder joints. Parylene (trademark of Union Carbide, chemical name Polyparaxylylene) and silicone conformal coating have been shown to improve accelerated fatigue life of SM solder joints by approximately a factor of two or three. However in thermal shock, some silicone coatings have been reported to decrease life in thermal shock.

7.0 ASSEMBLY PROCESSES AND DESIGN FOR MANUFACTURABILITY

While there are only a few processes used in fabricating an assembly with SMT components, these processes directly impact the formation of the solder joint that provides the reliable attachment of the part to the substrate. It is essential that the designer of surface mount assemblies understand the manufacturing processes involved, including their impact on the reliability of the completed assembly. Design for manufacturability requires that the designer have a clear view of the impact and limitations of the fabrication steps.

IPC-CM-770, Printed Board Component Mounting, includes the following classification scheme for surface mount assemblies:

Type 1 —Components (mounted) on only one side of

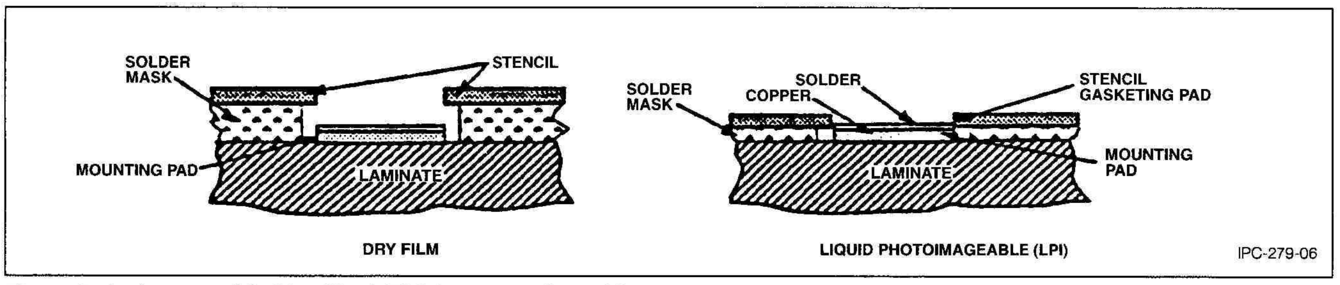


Figure 6–1 Impact of Solder Mask Thickness on Stenciling

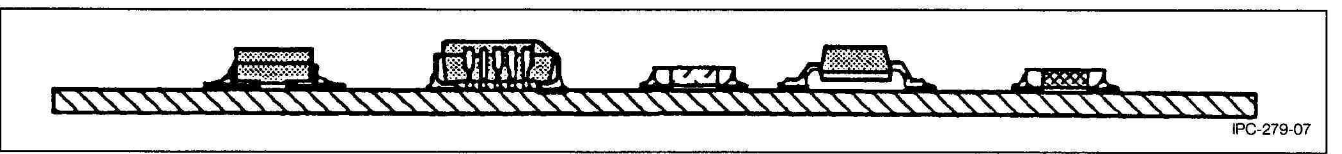


Figure 7–1 Type 1B Assembly – All SMT Components

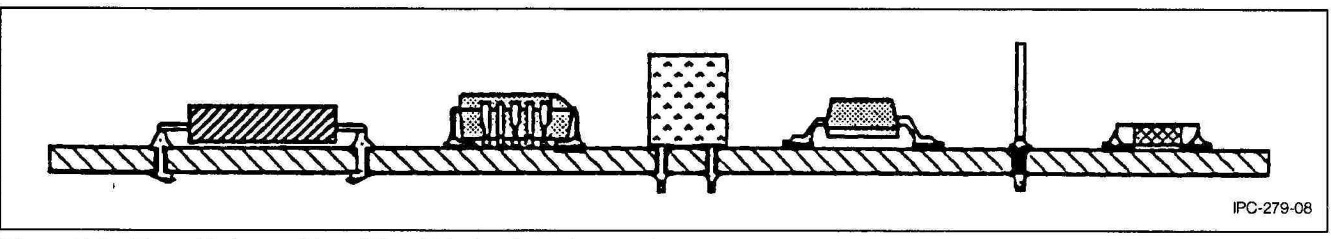


Figure 7–2 Type 1C Assembly – Mixed Technology Assembly

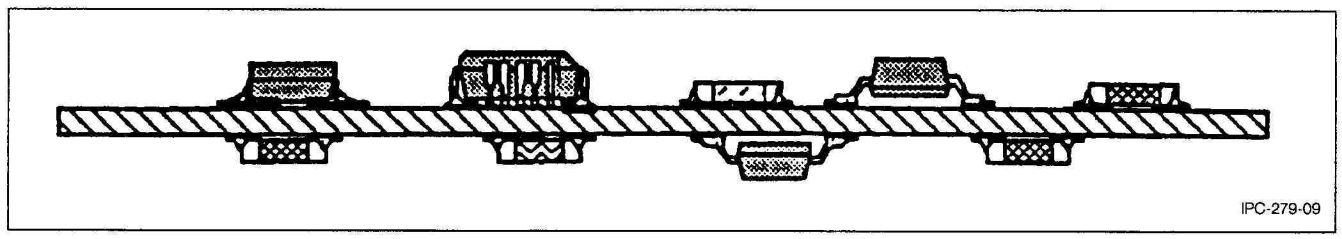


Figure 7–3 Type 2B – All SMT Components

the board

Type 2 —Components (mounted) on both sides of the board

Class A —Through-hole component mounting only

Class B —Surface mounted components only

Class C —A mixture of through-hole and surface mounting

The typical assembly with surface mount components on only one side of the substrate (Type 1B - Figure 7-1) is assembled by one of the following sequences:

1. Apply adhesive, place SM components, cure adhesive, wave solder, clean, test/repair.

or;

2. Apply solder paste, place SM components, reflow solder paste, clean, test/repair.

If the assembly contains both surface mount and through-hole components of a single-sided assembly (Type 1C Figure 7-2), it may be assembled using one of the following sequences:

1. Apply adhesive, place SM components, cure adhesive, wave solder, clean, insert through-hole components and clinch, wave solder, clean, test/repair.

or;

2. Apply solder paste, place SM components, reflow solder paste, clean, insert through-hole components and clinch, wave solder, clean, test/repair.

When only surface mount components are mounted on both sides of an assembly (Type 2B - Figure 7-3), there are typically two assembly options:

1. Apply solder paste to side 2 (bottom), place SM components, reflow solder paste, clean, invert board, apply solder paste to side 1 (top), reflow solder paste, clean, test/repair.

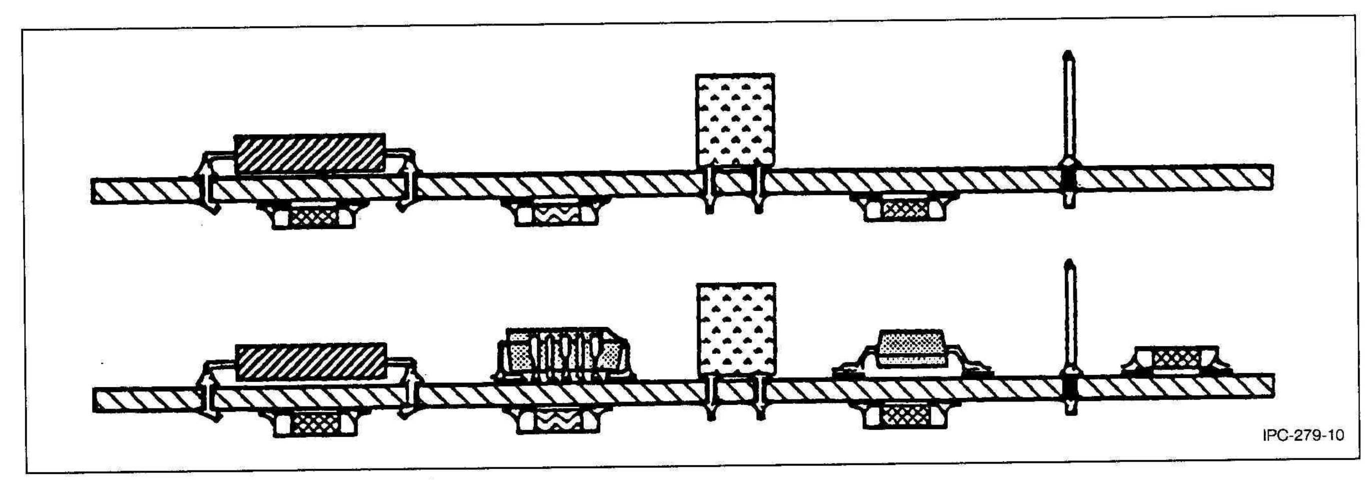


Figure 7–4 Type 2C – Mixed Technology

or;

2. Apply solder paste to side 2, dispense adhesive to side 2, place SM components, cure/bake adhesive/ paste, invert board, apply solder paste to side 1, place SM components, reflow solder paste, clean, test/ repair.

With mixed technology boards containing surface mounted and through-hole components on more than one side of the substrate (Type 2C - Figure 7-4), there are several typical sequence possibilities:

1. For SM components on side 2 only: Apply adhesive to side 2, place SM components, cure adhesive, clean, invert board, insert through-hole components and clinch, wave solder, clean test/repair.

or;

2. For SM components on both sides: Apply solder paste to side 1, place SM components, reflow solder paste, clean, invert board, apply adhesive to side 2, place SM components, cure adhesive, invert board, insert through-hole components and clinch, wave solder, clean, test/repair.
3. For SM components on both sides: Apply adhesive to side 2, place SM components, cure adhesive, apply solder paste to side 1, place SM components, reflow solder paste, clean, invert board, insert through-hole components and clinch, wave solder, clean, test/ repair.

or;

4. For SM components on both sides: Apply solder paste to side 1, place SM components, reflow solder paste, clean, insert through-hole components and clinch, apply adhesive to side 2, place SM components, cure adhesive, invert board, wave solder, clean, test/repair.

7.1 Solder Paste Application Solder paste may be applied to a substrate either by syringe application or screen/stencil printing. The first issue impacting reliability at this stage is the alloy composition of the solder paste being deposited. Solder comes in a variety of alloys including combinations of tin, lead, silver, antimony, bismuth, indium and cadmium. Each alloy has a distinct set of metallurgical properties and the selection should be based on compatibility with the metals being joined (including leaching and intermetallic formation), the service environment and the service/process temperatures. Reliability will also be affected by the type of flux system used in the solder paste; high reliability applications should be limited to the use of R (rosin) or halide-free RMA (rosin-mildly activated) types.

Another contributor to reliability in this assembly operation is the volume of solder paste deposited since it will dictate the size of the solder joint. Careful consideration should be given to parameters that will affect solder volume such as stencil thickness and aperture sizes, squeegee/syringe pressure, metal content of the solder paste and thickness of solder coating on the printed board or substrate. See Appendix M for details.

7.2 Adhesive Application Adhesive used to mount components for subsequent wave soldering is typically applied via a syringe dispensing method (either manual or automatic). The volume of deposited adhesive should be adequate to restrain the part in place but not impinge on land areas or affect solderability and solder joint formation. All adhesives should be tested for their tendency to form voids that can entrap flux and affect long term reliability. Adhesive voids may also be caused by curing the material too rapidly. Adhesives may outgas even after complete curing.

7.3 Component Placement The placement of components on the substrate may be accomplished either manually or by using a broad range of pick-and-place equipment. Accurate positioning of components to their

respective land areas is necessary for complete solder joint formation, and thereby contributes to solder joint reliability. Fully automated pick-and-place equipment requires the use of fiducials (which are designed into the bare printed board) for the accurate alignment of the components relative to the substrate. Fine pitch components often require their own set of fiducials near or inside the footprint to assure accurate placement. The type of fiducial (circle, cross, pound sign, etc.) that works best depends on the particular assembly equipment used. Refer to IPC-SM-782 for fiducial and land pattern information.

Bent and skewed component leads may also contribute to improper location of some leads relative to their corresponding pads, leading to solder wicking and incomplete solder joints. Checks for lead coplanarity are often done for high reliability assemblies.

For large volume manufacturing, the placement of smaller substrates in a panelized format with snap-out features or scored edges provides more efficient assembly and results in potentially less handling damage. Care must be taken to design these features correctly to prevent damage to solder joints and board interconnects upon separation of the individual assemblies from the panel.

7.4 Soldering

7.4.1 Solder Paste Reflow Solder paste reflow is typically performed by forced convection, infrared, vapor phase, or laser soldering process. Important parameters that will affect the reliability of the components and assembly include: heating ramp rate, peak temperature in preheat, time above the minimum reflow temperature (20°C above liquidus for copper), peak reflow temperature and cooling rate and duration above the glass transition temperature of the substrate. Control of the reflow profile is required to minimize damage to the components and printed board and to control the formation of intermetallic compounds at the solder-substrate interface. The formation of appreciable intermetallic compounds has been identified as one of the main sources of solder joint failure. See also IPC-SM-816.

High pin count, plastic leaded chip carriers, thin quad flat packs, thin small outline packages and small outline ICs (PLCCs, TQFP, TSOP, and SOICs) may exhibit cracking of the plastic package upon reflow. See 5.3.5 and Appendix F.6.

7.4.2 Wave Soldering The wave soldering of surface mount components requires that the parts be correctly oriented during the design phase. If this is not performed, the terminations may be soldered using specialized wave geometries (e.g. dual or vibrating wave), however, the trailing terminations will exhibit oversized solder fillets that may stress and crack chip components.

A good solder joint can form only if the flux has properly cleaned and prepared the surfaces for the molten solder. Therefore, activity of the flux is a parameter that needs close monitoring to prevent dewetted and nonwetted solder joints. As with reflow soldering, a good soldering profile is essential to reducing solder defects and preventing thermal shock cracking of chip capacitors.

The presence of contamination in the solder greatly impacts the appearance and integrity of the solder joint. Gold in sufficient quantities (> 3% by weight) can result in seriously embrittled joints. Solder bath contaminant levels should be regularly monitored and limited to the levels found in IPC-S-815.

Active plastic packages such as SOICs and PLCCs may be adversely affected by wave soldering if flux seeps into the lead frame. There is a potential for this to happen since the lead frame and molding compound have different coefficients of expansion. Passive components may exhibit leaching of the precious metal terminations during wave soldering. If dwell time in the solder wave is minimized (3-4 seconds), leaching on these parts can be prevented by a nickel barrier underplating between the precious metal adhesion layer and the solder coating.

7.5 Cleaning Due to the low clearance of many surface mount components, flux residues become entrapped underneath. Remaining flux may eventually cause corrosion and electrical malfunctioning, hence, complete removal of active flux residues are essential to long term reliability. Following soldering, it may be necessary to initiate immediate cleaning to prevent hardening of the flux that makes removal difficult. The effectiveness of the cleaning process should be monitored by measuring ionic residues. See the test procedures in J-STD-001.

Besides flux, it may be necessary to remove a range of other residues such as solder oils, dross particles, strippable solder mask materials, solder balls and particulate matter.

The cleaning medium (solvent) can adversely affect the solder mask, printed board, conformal coating, board or component legends/marking/labels, thin or mechanically stressed sections of plastic components. Appendix I discusses the specifics of solvent compatibility on various plastics and metals.

7.6 Rework/Repair Repair and rework equipment are typically one of two types: hot air devices and conductive tips. When hot air devices are used, care should be taken to prevent thermal damage to adjacent components and the surrounding area of the printed board. The number of times that a part is removed and replaced should be limited in order to prevent internal thermal damage such as interconnect separations within the substrate. Desoldering time when using conductive tips should be limited to three seconds to prevent thermal damage. See IPC-R-700 for rework and repair methods. See 7.8.1.2 for reliability impacts.

RO-L0, RE-L0, RO-L1 flux per J-STD-004 should be used during rework operations and the component should be cleaned immediately following rework. Compatibility of the flux used in repair/rework with the flux used in the original processing should be assumed prior to repair/ rework. Only RO-L0 or RE-L0 flux should be used in repair or rework of conformally coated assemblies as typically the conformal coating will not withstand exposure to cleaning processes necessary to completely clean activated flux (e.g., L1, formerly RMA or RA) flux residues. For no-clean manufacturing processes, no cleaning should take place following touchup or repair.

7.7 Depaneling Surface mount assemblies that have been panelized to facilitate handling during the assembly steps will eventually need to be removed from the panel for use. Depaneling may be required before or after electrical testing (based on the design of the test fixture). Individual board assemblies are typically attached together by webs of substrate material that are left following partial routing of the board outline. These webs may contain drilled holes to promote easy "snap-out" of the individual boards. Also common is the use of scoring (either from one or both sides) which produces a groove to assist with depaneling. It is also possible to completely rout the boards from the assembled panel.

The depaneling operation exerts large mechanical stresses throughout the substrate and assembly. Extreme care must be taken to limit these stresses so that their impact on the board interconnects and surface mount solder joints is minimized.

7.8 Design for Manufacturability

7.8.1 Components

7.8.1.1 Soldering Effects The design process must consider the effects of soldering on components in order to produce a reliable assembly.

Components that may be susceptible to degradation from thermal excursions caused by soldering include plastic film capacitors, pulse transformers, inductors, delay lines, passive networks, relays, crystals, and crystal oscillators. In some instances, insulative or reflecting heat shields may provide sufficient thermal isolation. Where the thermal limitations arise from other causes such as internal plastics with low melting or softening point (e.g., plastic film capacitors, light emitting diodes (LEDs)), or internal liquids with low boiling point (e.g., liquid electrolytic capacitors or batteries), internal plastics with high CTE, representing a large fraction of the package volume (e.g., silicon stress relief coating of pulse transformers, passive delay lines), or structural materials of low deflection temperature thermoplastic materials (e.g., connectors or sockets), the same general alternatives apply.

Where there are thermally massive components such as high pin count connectors, sockets, PGAs or PLCCs with affixed heatsinks, the process design review should include items such as adequate solder joint temperature, as well as overheating of adjacent smaller components.

Where there are laminated ceramic and ferrite components such as multilayer ceramic capacitors (MLCC), chip inductors, and filter networks, they should be characterized for the peak temperature in the process to be used and preheated for a thermal shock $\Delta T/\Delta t < 4°C$/second and a $\Delta T < 100°C$.

Where there are tall components next to short or low profile components, the process design review should check for thermal shadowing effects from overhanging portions of the taller components.

7.8.1.2 Rework and Repair Effects "Touch up" is the application of heat and solder to a solder joint which is deemed cosmetically imperfect. Rework is the correction of a defect before the SM PWA leaves the plant. Repair is the correction of a defect found in the field. Information on rework and repair may be found in IPC-R-700. Each correction requires the heating of one or more solder joints significantly above the liquidus temperature of lead-tin eutectic solder (183°C) and may involve the removal and replacement of a component. Note that this temperature of 183°C is well above several critical temperatures for the assembly.

These critical temperatures include the printed board glass transition temperature, the temperature at which intermetallic growth occurs, plastic encapsulation glass transition temperature for components, vapor pressure effects on plastic encapsulated components and printed boards, solder melt temperature, temperature excursion (ΔT) and temperature rate of change ($\Delta T/\Delta t$). See Appendix E for a discussion of the effects of exceeding critical temperatures.

8.0 TESTING

Surface mount technology assemblies consist of multiple, high pin count, complex components connected into one circuit with high density interconnections. With this massive increase in density over plated through hole designs, the SMT PWA must be designed for testability. Emerging technologies such as multichip module (MCM), tape automated bonding (TAB), and flip-chip depend on design for testability to be cost effective.

Testability is a design characteristic defined as the ease of testing or the ability to allow cost effective testing. Testability is a measure of the support which a system/module/ card/ component provides in fault detection and fault isolation. The greatest attention has been paid to digital testability. Previous techniques, including massive addition

of test nodes, become less feasible with the smaller dimensions of SMT PWAs and the number of test nodes required for components with 100-400 terminations; the mechanical force exerted by test pins is sufficient to flex and break components and solder joints. IEEE 1149.1 is the digital boundary scan standard; the proposed IEEE 1149.4 will be the analog testability bus standard.

Testability is a particular issue for field repair activities where the full capabilities of the SM PWA may not be exercised due to test equipment limitations or lack of available test time; Built-in-Test-Equipment, Built-in-Test, Built-in-Self-Test (BITE, BIT or BIST) capabilities could be invaluable in these circumstances.

Increased Testability leads to easier, less complex external testing with the following tradeoffs: cost savings associated with increased test fault coverage; shortened test development time; shortened test length/application time; shortened design verification time; reduced defect levels; reduced required tester memory and complexity; reduced test fixture complexity vs. increased costs associated with increased silicon/printed board area; increased number of I/O pins and connectors; increased circuit delay; increased power dissipation; increased design time.

The link between Testability and Design for Reliability for SMT PWAs lies in the provisions for fault detection and fault isolation at the system/SMT module/SMT card/SMT component levels for complex functions. Greater testability should lead to increased system availability through reduced time required for debugging/ trouble-shooting/ repair/ service/ maintenance. Additional benefits include fewer hard or intermittent failures discovered during system operation, fewer failures attributed to marginal performance, and shortened time for failure analysis to root cause.

8.1 Design for Testability (DfT) DfT is the deliberate effort to ensure the inherent testability of a circuit. At the chip, at the board level and at the assembly level, a circuit must be designed for test from the conception of design through its final gate level detail. Testability cannot be added effectively into a complex design after the design is complete. As the density of assemblies increase, manual board probing becomes less and less viable and board test requirements necessitate simulation modeling. The pressure on the hardware designer to reduce the product's Time to Market (TTM) requires that the techniques of Concurrent Engineering be used during product development to consider and implement appropriate Design for Testability measures.

The three goals in implementing testability are controllability, observability, and partitioning. Controllability is the ability to manipulate signal flow within a circuit. Observability is the measure of the extent to which signal activity can be monitored. Partitioning is the reduction of complex circuitry into a set of minimally interactive subcircuits. For details see Appendix J.

Designing for testability is best achieved through concurrent engineering, where test strategies are defined and incorporated into the design. The appropriate DfT technique may be the placement of adequate test pads for bare board and in-circuit test (ICT). Appropriate DfT technique may be the placement of adequate test pads for bare-board and in-circuit test (ICT). For ICT, supplemental jumpers to be connected or removed as part of the test routine may be required; for bare-board test, test pads at the end-of-net may be required to validate the integrity of PTH and via connections.

8.2 Testing Philosophy Testing is one means of decreasing defects in and increasing the reliability of SMT assemblies. The best strategy in design for testability is to plan for executing every test type available. This is achieved (on bare boards) by providing 100% access to every node of every net from either side of the board. Successful implementation of this strategy on complex, dense designs can be achieved if adopted at the beginning of the design phase.

Testing can be performed at the bare chip, component, bare substrate, and/or loaded substrate levels. The wide range in testing levels allows for detection and isolation of faults or defects at the earliest possible level. The types of fault categories detected include printed board fabrication faults, soldering faults, assembly errors, defective components, and functional failures.

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Fine Pitch Technology
Chip on Board Technology
Multichip Module Technology
Hybrids

Substrates:
Rigid Boards and Rigid Board Assemblies
Flexible Boards and Flexible Board Assemblies
Metal Core Boards

Process Parameters:
Statistical Process Control:
Process Control and Troubleshooting

Connectors and I/O Interconnection Adhesives:
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Insulative (Structural)
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9.17 Accelerated Life Testing

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9.18 Solder, Solderability, Soldered Assembly Quality

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Appendix A
Design for Reliability (DfR) of Solder Attachments

A-1.0 SURFACE MOUNT SOLDER ATTACHMENT RELIABILITY

The fatigue behavior of surface mount solder joints has been investigated experimentally in numerous studies. The results of the studies that were carried out in a manner to assure the same damage mechanism as the mechanism operative in typical electronic products have yielded a mathematical solder fatigue model. This model has been expanded and augmented to its current form, presented in this section, as additional test results became available.

The model is for uncoated solder attachments. The complexity and vast differences in conformal coatings make it impossible to develop a generic model that considers all the variables. Products with conformal coatings should be evaluated using test vehicles having the same coating and test vehicles without the coating in order to assess the impact of the coating on reliability.

A-2.0 DAMAGE MECHANISMS AND FAILURE

The reliability of electronic assemblies depends on the reliability of their individual elements and the reliability of the mechanical thermal, and electrical interfaces (or attachments) between these elements. One of these interface types, surface mount solder attachment, is unique since the solder joints not only provide the electrical interconnections, but are also the sole mechanical attachment of the electronic components to the printed board and often serve critical heat transfer functions as well.

A solder joint in isolation is neither reliable nor unreliable; it becomes so only in the context of the electronic components that are connected via the solder joints to the printed board. The characteristics of these three elements - component, substrate, and solder joint - together with the use conditions, the design life, and the acceptable failure probability for the electronic assembly determine the reliability of the surface mount solder attachment.

A-2.1 Solder Joints and Attachment Types

Solder joints are anything but a homogeneous structure. A solder joint consists of a number of quite different materials, many of which are only superficially characterized. A solder joint consists of:

(1) the base metal at the printed board
(2) one or more intermetallic compounds (IMC)—solid solutions—of a solder constituent—typically tin (Sn)—with the printed board base metal
(3) a layer from which the solder constituent forming the printed board-side IMC(s) has been depleted
(4) the solder grain structure, consisting of at least two phases containing different proportions of the solder constituents as well as any deliberate or inadvertent contaminations
(5) a layer from which the solder constituent forming the component-side IMC(s) has been depleted
(6) one or more IMC layers of a solder constituent with the component base metal, and
(7) the base metal at the component.

The grain structure of solder is inherently unstable. The grains will grow in size over time as the grain structure reduces the internal energy of a fine-grained structure. This grain growth process is enhanced by elevated temperatures as well as strain energy input during cyclic loading. The grain growth process is thus an indication of the accumulating fatigue damage. At the grain boundaries contaminants like lead oxides are concentrated; as the grains grow these contaminants are further concentrated at the grain boundaries, weakening these boundaries. After the consumption of ~25% of the fatigue life micro-voids can be found at the grain boundary intersections; these micro-voids grow into micro-cracks after ~40% of the fatigue life; these micro-cracks grow and coalesce into macro-cracks leading to total fracture as is schematically shown in Figure A-1.

Surface mount solder attachments exist in a wide variety of designs. The major categories are leadless and leaded solder attachments. Among the leadless solder joints a differentiation has to be made between those without fillets, e.g., Flip-Chip C4 (Controlled Collapse Chip Connection) solder joints, BGAs with C5 (Controlled Collapse Chip Carrier Connection) solder attachments, BGAs with high-temperature solder (e.g., 10Sn/90Pb) balls, and CGAs with high-temperature solder columns; and solder joints with fillets, e.g., chip components, Metal Electrode Face components (MELFs), and castellated leadless chip carriers. The leaded solder attachments differ primarily in terms of their compliancy and can be roughly categorized into components with super-compliant leads {K_D<~9 N/mm}, compliant leads (~9 N/mm<K_D<~90 N/mm), and non-compliant leads {(K_D>~90 N/mm}.

The different surface mount solder attachment types can have significantly different failure modes. Solder joints with essentially uniform load distributions, e.g., Flip-Chip, BGA, CGA, show behavior as illustrated in Figure A-1. Solder joints with non-uniform load distributions, e.g., those on chips components, MELFs, leadless chip carriers,

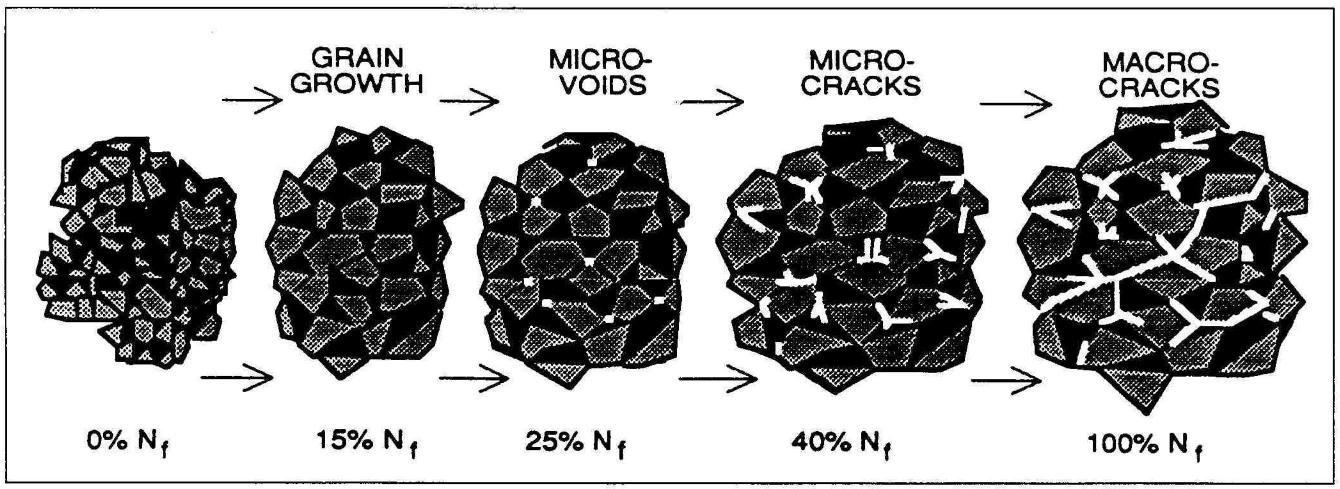


Figure A-1 Depiction of the Effects of the Accumulating Fatigue Damage in Solder Joint Structure

Table A-1 Realistic Representative(1) Use Environments, Service Lives, and Acceptable Failure Probabilities for Surface Mounted Electronics Attachments by Use Categories [Ref. A-9: 10]

	Worst-Case Environment						
Use Category	**Tmin °C**	**Tmax °C**	**ΔT(2) °C**	**Dwell Time t_D hrs**	**Cycles/Year**	**Typical Years of Service**	**Accept. Failure Risk(3), %**
Consumer	0	+60	35	12	365	1-3	~1
Computers	+15	+60	20	2	1460	~5	~0.1
Telecom	-40	+85	35	12	365	7-20	~0.01
Commercial Aircraft	-55	+95	20	12	365	~20	~0.001
Industrial and Automotive Passenger Compartment	–55	+96	20 &40 &60 &80	12 12 12 12	185 100 60 20	~10	~0.1
Military Grounds and Ship	–55	+95	40 &60	12 12	100 265	~10	~0.1
Space leo geo	–55	+95	3 to 100	1 12	8760 365	5-30	~0.001
Military Avionics a b c Maintenance	–55	+95	40 60 80 &20	2 2 2 1	365 365 365 365	~10	~0.01
Automotive under hood	–55	+125	60 &100 &140	1 1 2	1000 300 40	~5	~0.1

& = in addition
1 Does not cover all possible use environments, but only most common.
2 ΔT represents the maximum temperature swing, but does not include power dissipation effects for components; for reliability estimations the actual local temperature swings for components and substrate, including power dissipation should be used.
3 The 'Acceptable Failure Risk' is the percentage of product in the field that has failed, due to wearout mechanisms, at the end of the 'Typical Years of Service.'

and all leaded solder joints, show localized damage concentrations with the damage shown in Figure A-1 preceding an advancing macro-crack.

The solder joints frequently connect materials of highly disparate properties, causing global thermal expansion mismatches [Refs. A-9: 1-6], and are made of a material, solder, that itself has often properties significantly different than the bonding structure materials, causing local thermal expansion mismatches [Refs. A-9: 4,7].

The severity of these thermal expansion mismatches, and thus the severity of the reliability threat, depends on the design parameters of the assembly and the operational use environment. In Table A-1 guidelines as to the possible use environments for nine of the more common electronic applications are illustrated [Refs. A-9: 8,9]. However, it needs to be emphasized, that the information in Table A-1 should serve only as a general guideline; for some use categories the description of the expected use environment

can be rather more complex [Ref. A-9: 9].

A-2.2 Global Expansion Mismatch

The global expansion mismatches result from differential thermal expansions of an electronic component or connector and the printed board to which it is attached via the surface mount solder joints. These thermal expansion differences result from differences in the CTEs and thermal gradients as the result of thermal energy being dissipated within active components.

Global CTE-mismatches typically range from $\Delta\alpha \sim 2$ ppm/°C (1 ppm=1×10^{-6}) for CTE-tailored high reliability assemblies to ~14 ppm/°C for ceramic components on FR-4 printed boards. CTE-mismatches of $\Delta\alpha < 2$ ppm/°C are not achievable in reality as a consequence of the variability of the CTE values of the materials involved on both components and printed boards.

Global thermal expansion mismatches typically are the largest, since all three parameters determining the thermal expansion mismatch—the CTE-mismatch, $\Delta\alpha$, the temperature swing, ΔT, and the acting distance, L_D—are large.

This global expansion mismatch will cyclically stress, and thus fatigue, the solder joints. The cyclically cumulative fatigue damage will ultimately cause the failure of one of the solder joints, typically a corner joint, of the component causing functional electrical failure that is initially intermittent.

A-2.3 Local Expansion Mismatch

The local expansion mismatch results from differential thermal expansions of the solder and the base material of the electronic component or printed board to which it is soldered. These thermal expansion differences result from differences in the CTE of the solder and those of the base materials together with thermal excursions [Refs. A-9: 4,7].

Local CTE-mismatches typically range from $\Delta\alpha \sim 7$ ppm/°C with copper to ~18 ppm/°C with ceramic and ~20 ppm/°C with Alloy 42 and Kovar ™. Local thermal expansion mismatches typically are smaller than the global expansion mismatches, since the acting distance, the maximum wetted area dimension, is much smaller—in the order of hundreds of ~µm.

A-2.4 Internal Expansion Mismatch

An internal CTE-mismatch of ~6 ppm/°C results from the different CTEs of the Sn-rich and Pb-rich phases of the solder. Internal thermal expansion mismatches typically are the smallest, since the acting distance, the size of the grain structure, is much smaller than either the wetted length or the component dimension—in the order of less than 25 µm [Ref. A-9: 11].

A-2.5 Solder Attachment Failure

The failure of the solder attachment of a component to the substrate to which it is surface mounted is commonly defined as the first complete fracture of any of the solder joints of which the component solder attachment consists.

Given that the loading of the solder joints is typically in shear, rather than in tension, the mechanical failure of a solder joint is not necessarily the same as the electrical failure. Electrically, the mechanical failure of a solder joint results, at least initially, in the occasional occurrence of a short-duration (<1 µs) high-impedance event during either a mechanical or thermal disturbance. From a practical point of view, the solder joint failure is defined as the first observation of such an event.

For some applications this failure definition might be inadequate. For high-speed signals with sharp rise times signal deterioration prior to the complete mechanical failure of a solder joint might require a more stringent failure definition. Similarly, for applications which subject the electronic assemblies to significant mechanical vibration and/or shock loading, a failure definition that considers the mechanical weakening of the solder joints as the result of the accumulating fatigue damage might be necessary.

A-3.0 RELIABILITY PREDICTION MODELING

A-3.1 Creep-Fatigue Modeling

It has been experimentally shown [Refs. A-9: 2,4,12,13] that the fatigue life of surface mount solder joints can be described by a power law similar to the Coffin-Manson low-cycle fatigue equation [Ref. A-9: 14] developed for more typical engineering metals. For practical reasons and as the direct consequence of the time-dependent stress-relaxation/creep behavior of the solder at typical use environments (see Table A-1), the specialized case of the Coffin-Manson equation requires reversion to the more general strain-energy relationship of Morrow [Ref. A-9: 15]; it also requires that the cyclic strain energy be based on the total possible thermal expansion mismatch and that the exponent is a function of temperature and time to provide a measure of the completeness of the stress-relaxation process. The Engelmaier-Wild solder creep-fatigue equation [Refs. A-9: 1-6,9,12], subject to some caveats listed later, relates the cyclic visco-plastic strain energy, represented by the cyclic fatigue damage term, ΔD, to the median cyclic fatigue life for both isothermal-mechanical and thermal cycling [Ref. A-9: 16]

$$N_f(50\%) = \frac{1}{2}\left[\frac{2\epsilon'_f}{\Delta D}\right]^{\frac{-1}{c}} \qquad \text{[Eq. A-1]}$$

where

ϵ'_f = fatigue ductility coefficient, =0.325 for eutectic and 60/40 Sn/Pb solder (for other solders the value of ϵ'_f is expected to be somewhat different).

Solder, uniquely among the commonly used engineering metals, readily creeps and stress-relaxes at normal use temperatures; the rate of creep and stress-relaxation is highly temperature- and stress-level-dependent. Thus, the cyclic fatigue damage term, ΔD, for practical reasons, has to be based on the total potential damage at complete creep/ stress relaxation of the solder. For cyclic conditions that do not allow sufficient time for complete stress relaxation ΔD is larger than the actual fatigue damage. The temperature- and time-dependent exponent, c, compensates for the incomplete stress relaxation and is given by

$$c = -0.442 - 6x10^{-4} T_{SJ} + 1.74x10^{-2} \ln(1 + \frac{360}{t_D})$$

[Eq. A-2]

where
T_{SJ} = mean cyclic solder joint temperature
t_D = half-cycle dwell time in minutes.

The half-cycle dwell time relates to the cyclic frequency and the shape of the cycles and represents the time available for the stress-relaxation/creep to take place.

In Eq. A-1 the exponent is given as (−1/c), which is mentally confusing; this format exists for historical reasons in that the underlying work [Refs. A-9: 14,15] was always stated this way. For typical electronic applications (T_{SJ} = 0 to 100°C and t_D = 15 to 720 minutes) the exponent (−1/c ranges between 2.0 and 2.6.

Equations A-1 and A-2 come from a generic understanding of the response of SM solder joints to cyclically accumulating fatigue damage resulting from shear displacements due to the global thermal expansion mismatches between component and substrate. These shear displacements cause time-independent yielding strains and time-, temperature-, and stress-dependent creep/stress relaxation strains. These strains, on a cyclic basis, form a visco-plastic strain energy hysteresis loop which characterizes the solder joint response to thermal cycling and whose area, given as the damage term ΔD, is indicative of the cyclically accumulating fatigue damage. Hysteresis loops in the shear stress-strain plane have been experimentally obtained [Refs. A-9: 13,17-19].

A-3.2 Damage Modeling

The assessment of the cyclically cumulating fatigue damage is not a straight-forward task. While Eq. A-1 is widely used, the question of how to best quantify the cyclic fatigue damage is still hotly debated. The choices are primarily between more complex finite-element analyses (FEA), which can give more detailed information and can include second-order effects, but require a large number of not fully-supported assumptions [Ref. A-9: 20]; and closed-form empirically-based relationships of the first-order design parameters, which cannot include second-order effects and have use limitations due to their simple nature, but allow, due to their simple form, a direct assessment of the impact of the primary design parameters as well as design trade-offs.

The following cyclic fatigue damage terms are of the simplified closed-form type and should be utilized with the application caveats that follow [Refs. A-9: 1-6,9,12,16,21].

The cyclic fatigue damage term for leadless SM solder attachments, for which the stresses in the solder joints exceed the solder yield strength and cause plastic yielding of the solder, is

$$\Delta D(\text{leadless}) = \left[\frac{F L_D \Delta(\alpha \Delta T)}{h}\right]$$

[Eq. A-3]

For solder attachments with leads compliant enough, so that the solder joint stresses are below the yield strength and thus are not bounded by it, the cyclic fatigue damage term is

$$\Delta D(\text{leaded}) = \left[\frac{F K_D [L_D \Delta(\alpha \Delta T)]^2}{(919 \text{ kPa}) A h}\right]$$

[Eq. A-4]

where for English units the scaling coefficient is 133 psi instead of 919 kPa.

Equation A-4 contains the design parameters that have a first-order influence on the reliability of SM solder attachments. They are

A = effective minimum load bearing solder joint area;

F = empirical "non-ideal" factor indicative of deviations of real solder joints from idealizing assumptions and accounting for secondary and frequently intractable effects such as cyclic warpage, cyclic transients, non-ideal solder joint geometry, different solder crack propagation distances, brittle IMCs, Pb-rich boundary layers, and solder/bonded-material expansion differences, as well as inaccuracies and uncertainties in the parameters in Eqs. A-1 through A-4; 1.5>F> 1.0 for ball/column-like leadless solder joints (C4, C5, BGAs, CGAs), 1.2>F>0.7 for leadless solder joints with fillets (castellated chip carriers and chip components), F≈1 for solder attachments utilizing compliant leads;

h = solder joint height;

K_D = "diagonal" flexural stiffness of unconstrained, not soldered, corner-most component lead, determined by strain methods [see Refs. A-9: 22-25] or FEA;

L_D = maximum distance between component solder joints measured from component solder joint

pad centers, L_D is sometimes referred to as the distance from the neutral point (DNP);

T_C, T_S = steady-state operating temperature for component, substrate (T_C>T_S for power dissipation in component) during high temperature dwell;

$T_{C,0}$, $T_{S,0}$ = steady-state operating temperature for component, substrate during low temperature dwell, for non-operational (power off) half-cycles $T_{C,O} = T_{S,0}$;

T_{SJ} = $(1/4)(T_C+T_S+T_{C,O}+T_{S,O})$, mean cyclic solder joint temperature;

α_C, α_S = CTEs for component, substrate;

ΔD = potential cyclic fatigue damage at complete stress relaxation;

ΔT_C = $T_C-T_{C,O}$, cyclic temperature swing for component;

ΔT_S = $T_S-T_{S,O}$, cycling temperature swing for substrate (at component);

$\Delta(\alpha\Delta T)$ = $|\alpha_S\Delta T_S-\alpha_C\Delta T_C|$, absolute cyclic expansion mismatch, accounting for the effects of power dissipation within the component as well as temperature variations external to the component;

$\Delta\alpha$ = $|\alpha_C-\alpha_S|$, absolute difference in CTEs of component and substrate, CTE-mismatch, because of the inherent variability in material properties $\Delta\alpha<2x10^{-6}$ should not be used in calculating reliability.

A-3.3 CAVEAT 1 — Solder Joint Quality

The solder joint fatigue behavior and the resulting reliability prediction equations. Eqs. A-1 through A-2, were determined from thermal cycling results of solder joints that failed as a result of fracture of the solder, albeit sometimes close to the IMC layers. For solder joints for which layered structures are interposed between the base material and the solder joints, these equations could be optimistic upper bounds if the interposed layered structures become the 'weakest link' in the surface mount solder attachments. Such layered structures could be: metallization layers that have weak bonds to the underlying base material, or are weak themselves, or dissolve essentially completely in the solder; oxide or contamination layers preventing a proper metallurgical bond of the solder to the underlying metal; brittle IMC layers too thick due to too many or improperly long high temperature processing steps.

Some material choices can lead to lower quality and weaker solder joints because the material is more difficult to wet and solder. The nickel/iron alloys, Kovar™ and Alloy 42, fall into this material category. The resulting lower solder joint quality indicated in Table A-2 is also clearly evident in Figure A-2, where the solder joint pull strength is shown for a variety of differently prepared Alloy 42 and copper leads. Alloy 42 leads, even when etched or pre-flowed at temperatures higher than can be tolerated by the component, show a substantial reduction in the solder joint pull strength relative to copper. In the worst instance, the leads from one Alloy 42 manufacturer have a pull strength of less than half of those with more typical Alloy 42 and are essentially non-wettable.

Table A–2 Quality of Solder Joints with Copper and Alloy 42 Resulting from Different Reflow Temperatures

Reflow Temperature °C	Solder Joint Quality	
	60/40 Solder to Copper	60/40 Solder to Alloy 42
~210	just o.k.	marginal to bad
~240	good	just o.k.
~260	good	good

Early failures of the solder attachments of components with Alloy 42 lead frames and leads during accelerated testing [Refs. A-9: 26-30] and manufacture [Ref. A-9: 31] have been documented.

Solder joints which have solder joint heights (gaps) of h<50 to 75µm also require special attention. For solder joints that thin, the gap is essentially filled with intermetallic compounds and those solder metals that do not go into solution with the base metals to form the IMCs. Therefore Eqs. A-1 and A-2 do not apply because these gaps are not filled with solder [Ref. A-9: 32]. These materials do not creep as readily, if at all, at the prevailing temperatures and are typically more brittle, but much stronger than solder. Thus, fatigue lives are longer than would be predicted from Eqs. A-1 and A-2 unless overstress conditions occur.

On the other hand, the fatigue lives of solder attachments can be underestimated by Eqs. A-1 through A-4 if the component is underfilled with a load-bearing substance, e.g., epoxy [Ref. A-9: 33]. Components that are glued-down to the substrate result in higher solder joint fatigue reliability, since the solder joints are loaded in compression when the adhesive contracts on cooling from the solder reflow temperatures. Covercoats can either increase or decrease solder joint fatigue lives depending on the properties of the covercoat and when and how it is applied. Parylene™ has been found to increase the solder joint fatigue life by about a factor of three.

In general, caution might be indicated in all instances where the predicted life is less than 1000 cycles, because the severe loading conditions producing such short lives are likely to produce different damage mechanisms or/and failure modes.

A-3.4 CAVEAT 2 — Large Temperature Excursions

Solder joints experiencing large temperature swings (–50°C to + 80°C) which extend both significantly below and significantly above the temperature region bounded by

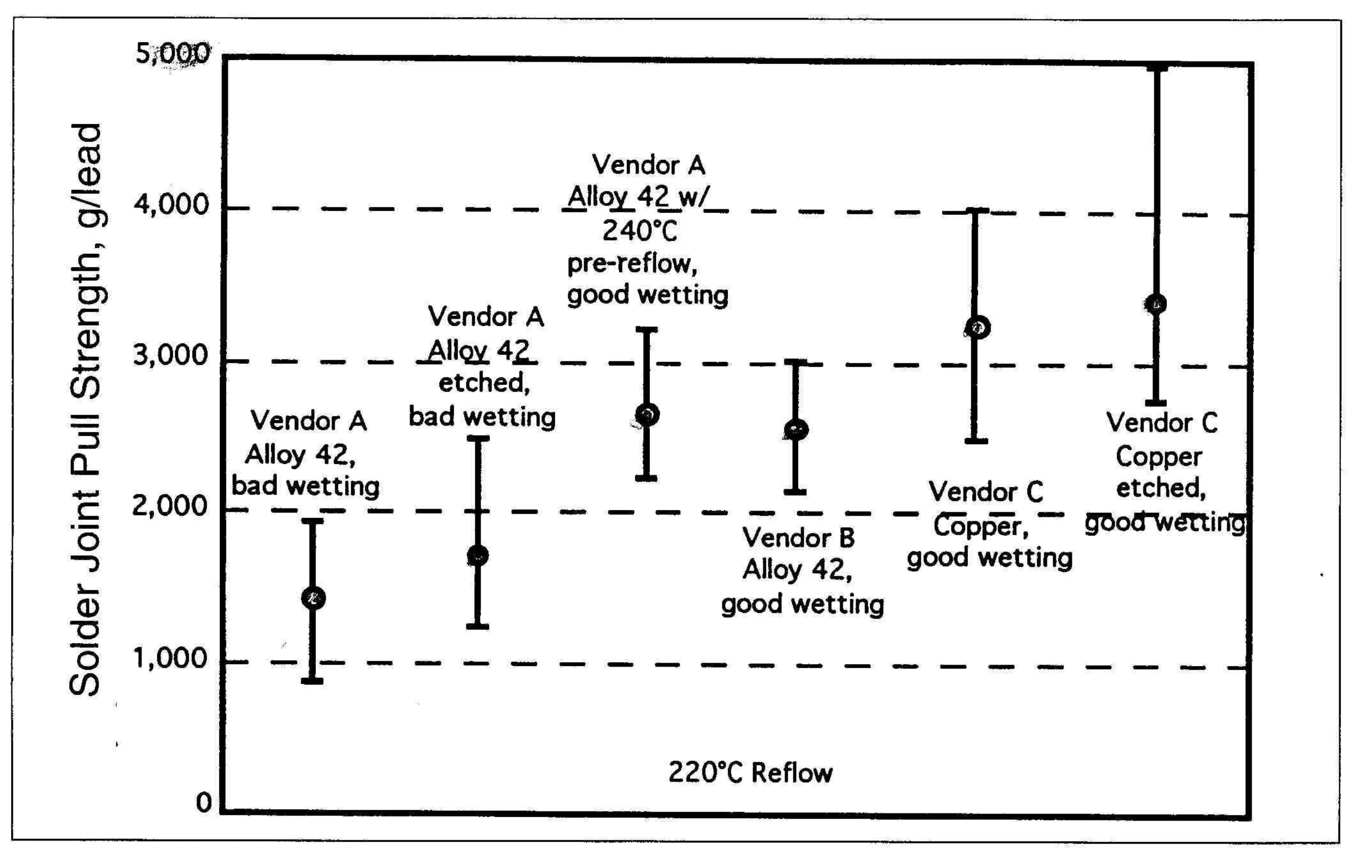


Figure A–2 Solder Joint Pull Strengths for Gullwing Leads Consisting of Alloy 42 from Different Vendors and Copper [Ref. A-9: 31]

−20°C to +20°C, in which the change from stress- to strain-driven solder response takes place, do not follow the damage mechanism described in Eqs. #1 and #2 [Ref. A-9: 34]. The damage mechanism is different than for more typical use conditions and is likely dependent on a combination of creep-fatigue, causing early micro-crack formation, and stress concentrations at these micro-cracks causing faster crack propagation during the high stress cold temperature excursions, as well as recrystallisation considerations.

A-3.5 CAVEAT 3 — High-Frequency/Low-Temperatures

For high-frequency applications, f>0.5 Hz or t_D<l s, e.g., vibration, and/or low temperature applications, $T_C < 0°C$, for which the stress relaxation and creep in the solder joint is not the dominant mechanism, the direct application of the Coffin-Manson [Ref. A-9: 14] fatigue relationship might be more appropriate. This relationship is

$$N_f(50\%) = \frac{1}{2}\left[\frac{2\epsilon_f'}{\Delta\gamma_p}\right]^{\frac{-1}{c}}$$

[Eq. A-5]

where $\Delta\gamma_p$ is the cyclic plastic strain range and $c \approx -0.6$.

It has to be noted, that the determination of $\Delta\gamma_p$ depends on the expansion mismatch displacements and the separation of the plastic from the elastic strains.

For loading conditions of this character, it is possible that high-cycle fatigue behavior may be observed.

A-3.6 CAVEAT 4 — Local Expansion Mismatch

For applications for which the global thermal expansion mismatch is very small, e.g. ceramic-on-ceramic or silicon-on-silicon (flip-chip solder joints), the local thermal expansion mismatch becomes the primary cause of fatigue damage. Equation A-4 does not address the local thermal expansion mismatch. This reliability problem needs to be assessed using an interfacial stress analysis [Ref. A-9: 35] and appropriate accelerated testing.

For leaded surface mount components with lead materials that have CTEs significantly lower than copper alloy materials, e.g., Kovar™ or Alloy 42, the results from Eqs. A-1 and A-2 will be optimistic, since the fatigue damage contributions from the solder/lead material CTE-mismatch, the local thermal expansion mismatch, are not included.

It has shown that the interfacial stresses resulting from the local expansion mismatch follow [Ref. A-9: 35].

$$\tau \propto L\,(\alpha_{Solder} - \alpha_{Basr})(T_{max} - T_{min})$$

[Eq. A-6]

where L is the wetted length of the solder joint. In addition, besides substantial shear stresses at the interface between the solder joint and the base material to which it is wetted, even larger peeling stresses occur. Both of these stresses are proportional to the parameters given in Eq. A-6.

From Eq. A-6 it is quite clear, that for leads consisting of Alloy 42, the wetted length of the solder joint, that is the length of the lead foot should be minimized to reduce interfacial stresses. That, of course, is contrary to the good practice that the foot length should be at least three times the lead width for optimum solder joint quality. However, since in most applications, the local expansion mismatch results in contributory damage to the more important damage caused by the global expansion mismatch, this contra-indication can be ignored without suffering catastrophic consequences.

From the available experimental data, the damage term, to be used in Eq. A-1, for the local expansion mismatch alone is

$$\Delta D(\text{local}) = \left[\frac{L\Delta\alpha\Delta T}{L_0}\right]$$

[Eq. A-7]

where the parameters are the same as in Eq. A-6 and L_0=0.1 mm, a scaling wetted length. The local expansion mismatch is then treated as an additional loading condition (see sections A-3.9 & A-3.10).

A.3.7 CAVEAT 5 — Very Stiff Leads/Very Large Expansion Mismatches

Equations A-3 and A-4 differentiate between surface mount solder attachments that are leadless and those with compliant leads. Leadless solder attachments presume substantial plastic strains due to yielding prior to creep and stress relaxation, whereas Eq. A-4 assumes that the compliant leads prevent stresses in the solder joints to reach levels where substantial yielding, and thus plastic strains prior to creep and stress relaxation, can take place.

However, there is an intermediate region that is not covered by these assumptions. For very stiff, non-compliant leads (e.g., SM connector headers), perhaps at lead stiffnesses K_D > ~90 N/mm and/or for very large thermal expansion mismatches (e.g., ceramic MCMs on FR-4) resulting in strain ranges $\Delta\gamma$ > ~10%, the damage estimates in Eq. A-4 can be substantially in error, because the assumptions underlying Eq. A-4 are violated.

For very stiff leads the stresses calculated in Eq. A-4 can exceed the yield strength of the solder. Since yielding will not permit stresses significantly higher than the yield strength, these calculated stress ranges will overestimate the cyclic fatigue damage and thus result in substantially underpredicted fatigue lives. To prevent this analytical error, the stress range in Eq. A-4 needs to be bounded by the yield strength of solder in shear.

For very large thermal expansion mismatches the full displacements will not be transmitted to the solder joints, because the leads will accommodate displacements by plastic deformations of the lead material. Possible exceptions are situations where very stiff leads are also involved, in which case the solder joint reliability is best estimated using Eq. A-1 for leadless solder attachments. The strain range that can be accommodated by creep and stress relaxation in the solder joints can be significantly exceeded by the displacements resulting from very large thermal expansion mismatches and the cyclic fatigue damage would be significantly overestimated. Under these conditions FEA is required to determine the split in the accommodation of the displacements between the lead and the solder joints.

Under these circumstances, Eqs. A-3 and A-4 will provide lower and upper bounds for the reliability estimates, respectively. The higher the lead stiffness, the closer the expected results will be towards the results given by Eq. A-3 for the leadless—'infinitely stiff leads'—solder attachments. Very high lead stiffnesses can occur in the case of through-hole component leads converted to surface mount and for connector headers where the male header pins have been simply bent into a gull-wing lead foot without any reduction in the lead cross-section. Very high thermal expansion mismatches occur primarily in accelerated testing and in extraordinary environments like storage and transport for products that are designed for benign operating environments.

A.3.8 Statistical Failure Distribution and Failure Probability

While the physical parameters define the median cyclic fatigue life from physics-of-failure considerations, solder attachment failures for a group of identical components will follow a distribution—like all fatigue results—which typically is best described by a Weibull statistical distribution [Ref. A-9: 36]. Given the statistical distribution, the fatigue life at any given failure probability for the solder attachment of a component can be predicted as long as the slope of the Weibull distribution is known. Thus, the fatigue life of surface mount solder attachments at a given acceptable cumulative failure probability per component, x, is —assuming a two-parameter (2P) Weibull statistical distribution—given by

$$N_f(x\%) = N_f(50\%)\left[\frac{\ln(1-0.01x)}{\ln(0.5)}\right]^{\frac{1}{\beta}}$$

[Eq. A-8]

where β = Weibull shape parameter or slope of the Weibull probability plot; typically $\beta\approx3$ for fatigue tests, from low-acceleration tests of stiff leadless solder attachments $\beta\approx4$ and ≈2 for compliant leaded attachments.

Experimentally, β can be found to be quite variable with more severely accelerated reliability tests resulting in tighter failure distributions and thus giving larger values for β. Values of β in the range of 1.8 to 9.0 have been observed.

There is some, unfortunately as yet inadequate, evidence that for lower failure probabilities a three-parameter (3P) Weibull distribution, postulating a failure-free period prior to first failure [Refs. A-9: 32,37], may be applicable. From physics-of-failure and damage mechanism considerations, a failure threshold as provided by a 3P-Weibull distribution makes sense, since the fatigue damage in the solder joints has to accumulate to crack initiation and complete crack propagation. While the 2P-Weibull distribution may be overly conservative for designs to very small acceptable failure probabilities ($x < \sim 0.1\%$), a too liberal choice of the failure-free period is definitely non-conservative. This area requires more work.

Also, when designing to low failure probabilities, the variability in the quality of the solder joints may no longer be negligible; also solder joints with latent defects that made it into the field will have in impact on the actual failure experience of a product in the field.

A-3.9 Multiple Cyclic Load Histories

The loading histories over the life of a product frequently include many different use environments and loading conditions [Refs. A-9: 38,39]. Multiple cyclic load histories (e.g., "Cold" temperature fatigue cycles combined with higher temperature creep/fatigue cycles (see Table A-1) combined with vibration and local expansion mismatches) all make their contributions to the cumulative fatigue damage in solder joints. Under the assumption that these damage contributions are linearly cumulative—this assumption underlies Eqs. A-1 and A-2 as well—and that the simultaneous occurrence or the sequencing order of these load histories makes no significant difference, the Palmgren-Miner's rule [Ref. A-9: 40] can be applied.

Frequently the initial reliability objective is stated as an allowable net cumulative damage ratio (CDR). The CDR is calculated as the sum of the ratios of the number of occurring load cycles to the fatigue life at each loading condition and is

$$CDR = \sum_{j=1}^{j} \frac{N_j}{N_{fj}} < 1$$

[Eq. A-9]

where

N_j = actual applied number of cycles at a specific cyclic load level j,

N_{fj} = fatigue life at the same specific cyclic load level j alone.

The fatigue life is frequently not completely specified and is normally taken to be the mean cyclic fatigue life. Equation A-8 can be used with the allowable CDR significantly less than unity to provide margins of safety, or more accurately, margins of ignorance.

Because the failure of solder joints results from wearout due to fatigue, the failure rate is continuously increasing. This is in stark contrast to the reliability design philosophy of MIL-HDBK-217 [Ref. A-9: 41] which presumes a constant failure rate. These increasing failure rates are properly represented by an appropriate statistical failure distribution.

Thus, to assure low failure risks, the fatigue life should be specified at the acceptable cumulative failure probability at the end of the design life as per Eq. A-3. Thus, Eq. A-9 is more appropriately written as

$$CDR(x\%) = \sum_{j=1}^{j} \frac{N_j}{N_{fj}(x\%)} = 1$$

[Eq. A-10]

where

$CDR(x\%)$ = cumulative damage ratio resulting in a cumulative failure probability of x%,

$N_{fj}(x\%)$ = fatigue life at the cyclic load level j and a failure probability of x% .

This approach works very well for the design of the solder attachment for a single component. However, it is inadequate for a reliability analysis of the whole assembly.

See section 3.1.13 for a discussion of non-linear or overload effects.

A-3.10 System Reliability Evaluation

Equations A-1 through A-10 address the reliability of the SM solder attachment of individual components. Systems consist of a variety of different components most of which occur in multiple quantities. Further, as shown in Table A-1, many use environments cannot and should not be represented by a single thermal cyclic environment, and accumulating fatigue damage from other sources, such as cyclic thermal environments as described in Caveats 2 to 4 as well as vibration, needs to be included also.

For a multiplicity of components, i, in the system, the effect of the various components on the system reliability can be determined from

$$F_{\Sigma}(N) = 1 - \exp\left\{ \ln(1 - 0.01x) \sum_{i=1}^{i} n_i \left[\sum_{j=1}^{j} \frac{N_{ij}}{N_{f,i,j}(x\%)} \right]^{\beta_i} \right\}$$

[Eq. A-11]

where

$F_\Sigma(N)$ = system cumulative failure probability after N total cycles,

n_i = number of components of type i,

$N_{i,j}$ = actual number of cycles applied to component i at a specific cyclic load level j,

$N_{f,i,j}$ (x%) = fatigue life of solder attachment of component i at load level j at x% failure probability,

β_i = Weibull slope for SM solder attachment of component i.

A-4.0 DfR-PROCESS

Appropriate DfR-measures to improve reliability can take one of two forms, which are best employed in combination for improved reliability margins. These measures are:

1) CTE-tailoring to reduce the global expansion mismatch;
2) Increasing attachment compliancy, e.g., by increasing the solder joint height, to accommodate the global expansion mismatch;
3) Underfilling the gap between the component and substrate;

Further, a DfR procedure aiming at high-reliability should also include

4) Choosing base materials that have not too large a local CTE-mismatch with solder, or
5) In case item (4) cannot be done, reduce the continuous wetted length to reduce interfacial stresses.

CTE-tailoring involves choosing the materials or material combinations of the MLB and/or the components to achieve an optimum ΔCTE. An optimum ΔCTE for active components dissipating power is ~1-3 ppm/°C (depending on the power dissipated) with the MLB having the larger CTE, and 0 ppm/°C for passive components. Of course, since an assembly has a multitude of components, full CTE-optimization cannot be achieved for all components—it needs to be for the components with the largest threat to reliability. For military applications with the requirement of hermetic—and thus ceramic—components, CTE-tailoring has meant the CTE-constraining of the MLBs with such materials as Kevlar™ and graphite fibers, or copper-Invar-copper and copper-molybdenum-copper planes. Such solutions are too expensive for most commercial applications for which glass-epoxy or glass-polyimide are the materials of choice for the MLBs. Thus, CTE-tailoring has to take the form of avoiding larger size components that are either ceramic (CGAs, MCMs), plastic with Alloy 42 leadframes (TSOPs, SOTs), or plastic with rigid bonded silicon die (PBGAs).

Increasing attachment compliancy for leadless solder attachments means increasing the solder joint height (C4, C5, shimming, gluing [Refs. A-9: 42,43], 10Sn/90Pb balls, 10Sn/90Pb columns) or switching to a leaded attachment technology. For leaded attachments, increasing lead compliancy can mean changing component suppliers to those having lead geometries promoting higher lead compliancy or switching to fine-pitch technology.

The DfR-process needs to emphasize a physics-of-failure perspective without neglecting the statistical distribution of failures. The process might involve the following steps:

A. Identify Reliability Requirements—expected design life and acceptable cumulative failure probability at the end of this design life;

B. Identify Loading Conditions—use environments (e.g., IPC-SM-785) and thermal gradients due to power dissipation, which may vary and produce large numbers of mini-cycles (Energy Star);

C Identify/Select Assembly Architecture—part and substrate selections, material properties (e.g., CTE), and attachment geometry;

D. Assess Reliability—determine reliability potential of the designed assembly and compare to the reliability requirements using the approach shown here, a 'Figure of Merit'-approach [Ref. A-9: 44], or some other suitable technique; this process may be iterative;

E. Balance Performance, Cost and Reliability Requirements.

A-5.0 CRITICAL FACTORS FOR EMERGING ADVANCED TECHNOLOGIES

The lessons learned over the past 15 years with surface mount technology (SMT) and fine-pitch attachments should be heeded and applied. However, some of the emerging advanced technologies fall outside the previous experience with SMT attachments. It is therefore important that appropriate design validation and qualification tests be carried out to extend and, if necessary, alter and augment, the existing understanding.

Following are short descriptions of some new technologies where DfR, particularly for the solder attachments, is of prime concern.

A-5.1 Flip Chip on Laminate

Here the biggest reliability concern is the large expansion mismatch between the chip silicon and the polymeric substrate. This either means relatively small chips or the use of organic underfill materials which relieve the solder joints from most of the thermal expansion mismatch loads. The underfill material does however make repairs difficult if not impossible. Detailed information about this technology has been assembled in ANSI/J-STD-012, Implementation of Flip Chip and Chip Scale Technology.

A-5.2 Area Arrays (BGA, CGA)

Grid array components (GACs) come in a variety of styles and materials. The major variations are BGAs, available with plastic bodies as PBGAs or ceramic bodies as CBGAs, and solder attached with either the C5-process or with solder joints containing 10Sn/90Pb solder balls; and CGAs with 10Sn/90Pb solder columns.

The long-term reliability of the solder attachments to FR-4 printed boards is a big concern with GACs. The global thermal expansion mismatch between the GACs and the printed board can be quite large as the result of the combination of large GAC sizes, large differences between the thermal expansion coefficients of the GACs and the printed board (ΔCTE), and the power dissipation within the GACs. Further, depending on the die attach and the GA material, a large localized global thermal expansion mismatch underneath the die and a significant local thermal expansion mismatch between the solder itself and the GA surface can increase the threat to reliability. In addition, the implementation of the Government-mandated "Energy Star" program, the number of thermal cycles could be a multiple of the once-a-day diurnal/on-off cycles.

The solder attachments of GACs vary depending on the loading conditions to which the solder joints are subjected to and the reliability requirements for the product. As mentioned earlier, BGAs are attached with either the C5-process or with 10Sn/90Pb solder balls. The C5-process, similar to the C4- or flip-chip-process, results in solder joints heights that are less controlled and lower {h~400 to 640 μm}, while the 10Sn/90Pb solder balls typically with diameters of 760 to 890 μm result in uniform solder joint heights of the same dimension since the 10Sn/90Pb solder has a liquidus temperature significantly above the near-eutectic Sn/Pb solders and does not melt during a typical reflow process. The solder columns, which currently are only used for ceramic GACs, are 10Sn/90Pb columns with lengths of 1.25 to 2.30 mm that are either cast onto the CGA or are wires soldered to both the CGA and the substrate with near-eutectic Sn/Pb solder. The ratios of fatigue lives, all parameters other than the solder joint height being equal, are CBGA(0.40 mm): CBGA(0.75 mm): CGA(2.30 mm) = 1: 4: 45. The height of the solder columns is limited by the requirement that the column height-to-diameter aspect ratio does not produce slender columns thus changing the loading conditions; cast columns can accommodate larger aspect ratios.

It is also of importance for PBGAs, how the silicon chips are attached to the BGA body. For 'cavity-up' components, only a thin plastic layer separates the solder joints from the die attach. As a consequence, the CTE underneath a rigid die attach can be as low as 6 to 8 ppm/°C (very similar to ceramic) locally raising the CTE-mismatch between the PBGA and the FR-4 printed board from ~2 to 10 ppm/°C. Thus, the die size can only be ~⅕ the size of the BGA to not negatively affect the reliability. Typically, die sizes are significantly larger than that, with the result that the solder joints at the corners of the die fail before the outermost BGA corner joints. The larger the die, the worse the solder attachment reliability [Refs. A-9: 45,46]. Thus, the trend towards perimeter-PBGAs, where solder joints exist only on the package perimeter—with the possible exception of some thermal solder balls and vias in the package center—for routing reasons, is beneficial for reliability [Ref. A-9: 47].

Further, the solder joint fractures are typically near the interface between the BGA and the barrel-shaped solder joints; this is a consequence of the contribution to the solder joint loading of the local expansion mismatch between the solder and the die-constraint BGA body [Ref. A-9: 45]. Substantial increases in fatigue life have reported with a soft die attach [Ref. A-9: 48].

The geometry of the solder joints as well as the solder land metallization have significant influence on the reliability. The solder masks can have a negative influence if they are used for solder mask-defined (SMD) lands with the solder mask on the metallization lands affecting the solder joint geometries. Stress concentrations created by the SMD-solder joint geometries can be the origin of solder joint failures and reduced reliability. For equal solder joint height, increases in fatigue life by factors of about 1.25 to 3 can be anticipated with the use of non-solder mask-defined (NSMD) vs. SMD lands with the larger improvements for solder joints with the more severe loading conditions [Refs. A-9: 46, 48-51].

For PBGAs the additional reliability issue of via and conductor failures has surfaced [Ref. A-9: 52]. The former issue is addressed in Section A-4 and the latter can be remedied by wider conductors and/or better copper foil [Ref. A-9: 53].

Detailed information about this technology has been assembled in ANSI/J-STD-013, Implementation of Ball Grid Array and Other High Density Technology.

A-5.3 Thin Packages (TSOP)

The biggest reliability issue regarding TSOPs (thin small outline packages) stems from the choice of Alloy 42 for the leadframe material by some component manufacturers [Refs. A-9: 27-31]. This material choice has the following consequences with regard to the solder attachment reliability:

(1) Increases global CTE-mismatch, because component CTE is reduced to about the CTE of ceramic;

(2) Increases lead stiffness due to higher modulus of elasticity reducing the effectiveness of the leads to

protect the solder joints from expansion mismatches;

(3) Reduces solder joint strength because of weaker solder/Alloy 42 interfacial bond (see Section A-3.3);

(4) Reduces solderability (see Section A-3.4).

These potential reliability-threats can be avoided with the choice of a copper lead frame; however, this requires a soft die attach and the reversion to higher CTE molding compounds for the components [Ref. A-9: 31].

perature and internal power cycling—is necessary.

A-7.0 SCREENING PROCEDURES

A-7.1 Solder Joint Defects

The solder joint defects of greatest reliability concern are those involving inadequate wetting for whatever reason. Well wetted solder joints, regardless of their geometric variations within the standards provided by IPC-A-620, Acceptability of Electronic Assemblies with Surface Mount Technologies and ANSI/J-STD-001, Requirements for Soldered Electrical and Electronic Assemblies, and somewhat beyond, will not pose a reliability threat due to inadequate quality. In Figure A-3 the results of thermal cycling and thermal shock tests are shown for solder joints of chip components with a wide variety of component offsets and overhangs.

Those solder joints have adequate strength even for severe mechanical loading conditions as well as no diminished thermal cyclic fatigue reliability. Only with severe offsets

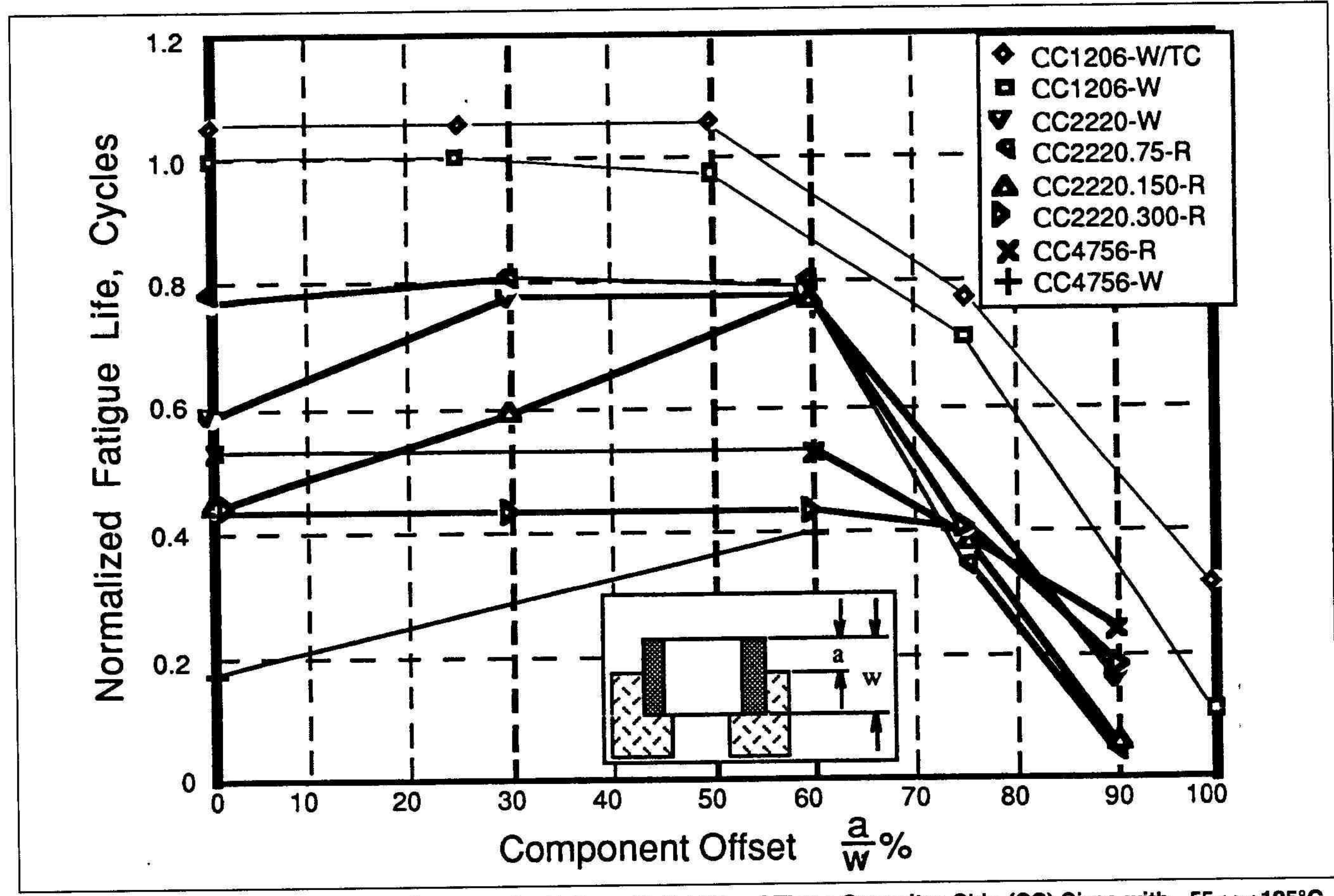


Figure A-3 Effect of Component Offsets on the Fatigue Reliability of Three Capacitor Chip (CC) Sizes with -55<->+125°C Thermal Shock or -20<->+100°C Thermal Cycling (TC) and Either Wave (W) or Reflow Soldered R) [Ref. A-9: 54,55]]. The Lower Lives at Smaller Component Offsets Result from the Failure of the CC-Components not the Solder Joints. The Fatigue Lives are Normalized, Since the Data are from Glued-Down CCs which Typically Exhibit Longer Solder Joint Fatigue Lives than CCs not Glued-Down.

A-6.0 VALIDATION AND QUALIFICATION TESTS

The validation and qualification tests should follow the guidelines given in IPC-SM-785, Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments.

However, for large components with significant heat dissipation and small global CTE-mismatches, temperature cycling tests are inadequate to provide the required information; full functional cycling—including external tem-

beyond Class 2 requirements is the reliability diminished. However, solder joints not properly wetted, can prematurely fail both as the result of mechanical and thermal cyclic loading [Refs. A-9: 1,31].

Voids in the solder joints are generally regarded as not constituting a reliability threat [Ref. A-9: 48]. Possible exceptions are large voids reducing the solder joint cross-section enough to reduce a required thermal heat transfer function, and voids in high-frequency applications where the voids can cause signal deterioration.

A-7.2 Screening Recommendations

Effective screening procedures need to be capable of causing the failure of latent solder joint defects, i.e., weak inadequately wetted solder joints, without causing significant damage to high quality solder joints.

The best recommendation is random vibration (6-10 grams for 10-20 minutes), preferably at low temperature, e.g., -40°C. This loading does not damage good solder joints, but overstresses weakly bonded ones [Ref. A-9: 1].

Thermal shock can also be successfully used, however some damage to good solder joints can be expected, particularly for larger components.

A-8.0 STEP-BY-STEP NUMERICAL EXAMPLE RELATING REQUIRED DESIGN LIFE TO ACCELERATED RELIABILITY TEST RESULTS

This numerical example illustrates how the reliability of an electronic system in the field can be assessed by using the Design for Reliability (DfR) process in Appendix A or the results of accelerated test results carried out as per IPC-SM-785, Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments.

For example the following information is assumed:

Product:

Computer for Navy artillery—Use Category 6 in Table A-1,

Design life = 10 years (= 3650 thermal cycles at 1 cycle/day),

Component-external daily temperature cycles: 45 to 85°C (ΔT = 40°C) for 100 days/year and 25 to 85°C (ΔT = 60°C) for 265 days/year (in the following text, the data and results for these two loading conditions appear before and after "//" respectively),

Acceptable cumulative failure probability at end of 10 years, x = 0.5%,

Largest leaded component:

68 I/O 50-mil pitch ceramic chip carrier (LCCC), α_C = 6.3 ppm/°C ($6.3x10^{-6}$/°C), dissipating 0.8 W raising the component operating temperature to 93°C, with side-brazed copper alloy compliant leads with a diagonal lead stiffness of K_D = 52 lb/in,

Largest leadless component:

CC1820 chip capacitor, α_C = 6.8 ppm/°C,

Substrate:

Low CTE multilayer board, α_S = 10.5 ppm/°C.

Reliability Estimates for Individual Components:

Ceramic Chip Carrier:

The input parameters into Eq. A-4 are: F = 1.0, K_D = 52 lb/in, L_D = 0.674 in, $\Delta(\alpha\ \Delta T)$ = $117.6x10^{-6}$//$201.6x10^{-6}$ (α_C = 6.3 ppm/°C, α_S = 10.5 ppm/°C, T_C = 93°C, T_S = 85°C, $T_{C,0}$ = $T_{S,0}$ = 45//25°C), A = $900x10^{-6}$ in^2, h = 0.005 in;

-> ΔD(leaded) = $5.459x10^{-4}$//$1.604x10^{-3}$ at ΔT = 40//60°C, respectively.

The input parameters into Eq. A-2 are: T_{SJ} = 67//57°C (T_C = 93°C, T_S = 85°C, $T_{C,0}$ = $T_{S,0}$ = 45//25°C), t_D = 715 min;

-> c = –0.4751//–0.4691 at ΔT = 40//60°C, respectively..

Using these results in Eq. A-1 gives:

=> N_f(50%) = 1,490,000//181,000 cycles at ΔT = 40//60°C, respectively.

Using these results in Eq. A-8 with x = 0.5% and β = 2 gives:

=> N_f(0.5%) = 127,000//15,400 cycles at ΔT = 40//60°C, respectively.

CC1820 Chip Capacitor:

The input parameters into Eq. A-3 are: F = 0.7, L_D = 0.080 in, $\Delta(\alpha\ \Delta T)$ = $148.0x10^{-6}$ (α_C = 6.8 ppm/°C, α_S = 10.5 ppm/°C, T_C = 85°C, T_S = 85°C, $T_{C,0}$ = $T_{S,0}$ = 45//25°C), h = 0.005 in;

-> ΔD(leadless) = $1.658x10^{-3}$//$2.486x10^{-3}$ at ΔT = 40//60°C, respectively.

The input parameters into Eq. A-2 are: T_{SJ} = 65//55°C (T_C = 85°C, T_S = 85°C, $T_{C,0}$ = $T_{S,0}$ = 45//25°C), t_D = 715 min;

-> c = –0.4739//–0.4679 at ΔT = 40//60°C, respectively.

Using these results in Eq. A-1 gives:

=> N_f(50%) = 148,000//73,000 cycles at ΔT = 40//60°C, respectively.

Using these results in Eq. A-8 with x = 0.5% and β = 4 gives:

=> N_f(0.5%) = 43,000//21,000 cycles at ΔT = 40//60°C, respectively.

Cumulative Damage Ratios for Multiple Cyclic Loads

The input parameters into Eq. A-10 are: N(ΔT = 40//60°C) = 1000//2650 cycles, N_f(0.5%, LCCC, ΔT = 40//60°C) = 127,000//15,400 cycles, N_f(0.5%, CC1820, ΔT = 40//60°C) = 43,000//21,000 cycles,

=> CDR(0.5%, LCCC) = 0.18 and CDR(0.5%, CC1820) = 0.15.

Reliability Estimates for Product with Multitude of Components:

The input parameters into Eq. A-11 are: x = 0.5%, N(ΔT =

40//60°C) = 1000//2650 cycles, n(LCCC) = 30, N_f(0.5%, LCCC, ΔT = 40//60°C) = 127,000//15,400 cycles, β(LCCC) = 2, n(CC1820) = 100, N_f(0.5%, CC1820, ΔT = 40//60°C) = 43,000//21,000 cycles, β(CC1820) = 4;

=>F_Σ(N = 3650) = 0.5%.

Thus, this design would just meet the reliability requirement of x ≤0.5% at the end of 10 years of service.

Accelerated Testing:

Test Components:

8 chip carriers (LCCC), 68 I/O 50-mil, α_C = 6.3 ppm/°C (measured), internally daisy-chained to allow independent monitoring of each LCCC side (¼ of LCCC), with side-brazed copper alloy compliant leads with a diagonal lead stiffness of K_D = 52 lb/in (calculated), 256 chip capacitors CC1820, α_C = 6.8 ppm/°C (measured), with metallization caps shorted with conductive epoxy on capacitor top,

Test Substrate:

FR-4 multilayer board, α_S = 16.0 ppm/°C (measured) for greater CTE-mismatches and greater test acceleration, test printed board lay-out provides for independent continuity monitoring of each side of each chip carrier (LCCC) and for continuity monitoring of groups of 8 chip capacitors (CCs) daisy-chained together. Conformal Coating: Test vehicles are not conformally coated.

Test Parameters:

Temperature cycling from 0°C to 100°C at 24 cycles/day, t_D = 15 min, ΔT = 100°C and T_{SJ} = 50°C.

Results of Accelerated Reliability Test:

	Cycles-To-Failure for Daisy-Chains							
Failure No.	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
¼ LCCC	146	196	388	418	486	540	568	628
8 CC1820	2718	3463	3826	4161	4397	4631	4738	5022
Failure No.	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**
¼ LCCC	676	684	690	820	850	878	902	926
8 CC1820	5206	5372	5489	5598	5823	5978	6073	6223
Failure No.	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
¼ LCCC	1038	1044	1096	1122	1206	1214	1298	1350
8 CC1820	6397	Test terminated at 6,400 cycles						
Failure No.	**25**	**26**	**27**	**28**	**29**	**30**	**31**	**32**
¼ LCCC	1386	1480	1536	1602	1716	1840	2002	2432
8 CC1820	Test terminated at 6,400 cycles							

N_f(50%) = 982 and 6310 accelerated cycles-to-failure for the individual LCCC sides and the 8 daisy-chained CC1820s, respectively. Applying the partition correction from Equation 16 in IPC-SM-785 results in N_f(50%) = 491 and 10612 accelerated cycles-to-failure for the actual LCCC and the CC1820 component attachments, respectively.

Reliability Estimates by Extrapolation of Accelerated Test Results:

Ceramic Chip Carrier:

The input parameters into Eq. A-4 are for the test: F = 1.0, K_D = 52 lb/in, L_D = 0.674 in, $\Delta(\alpha\,\Delta T)$ = 970.0x10^{-6} (α_C = 6.3 ppm/°C, α_S = 16.0 ppm/°C, $T_C = T_S$ = 100°C, $T_{C,0} = T_{S,0}$ = 0°C), A = 900x10^{-6} in^2, h = 0.005 in;

-> ΔD(test) = 3.714x10^{-2}.

and for the field use: F = 1.0, K_D = 52 lb/in, L_D = 0.674 in, $\Delta(\alpha\,\Delta T)$ = 117.6x10^{-6}//201.6x10^{-6} (α_C = 6.3 ppm/°C, α_S = 10.5 ppm/°C, T_C = 93°C, T_S = 85°C, $T_{C,0} = T_{S,0}$ = 45//25°C), A = 900x10^{-6} in^2, h = 0.005 in;

-> ΔD(use) = 5.459x10^{-4}//1.604x10^{-3} at ΔT = 40//60°C, respectively.

The input parameters into Eq. A-2 are for the test: T_{SJ} = 50°C ($T_C = T_S$ = 100°C, $T_{C,0} = T_{S,0}$ = 0°C), t_D = 15 min;

-> c(test) = –0.4160;

and for the field use: T_{SJ} = 67//57°C (T_C = 93°C, T_S = 85°C, $T_{C,0} = T_{S,0}$ = 45//25°C), t_D = 715 min;

-> c(use) = –0.4751//–0.4691 at ΔT = 40//60°C, respectively.

Using these results in Eq. A-12 in IPC-SM-785 with N_f(test, 50%) = 491 cycles gives:

=> N_f(use, 50%) = 1,500,000//183,000 cycles at ΔT = 40//60°C, respectively.

CC1820 Chip Capacitor:

The input parameters into Eq. A-3 are for the test: F = 0.7, L_D = 0.080 in, $\Delta(\alpha\,\Delta T)$ = 920.0x10^{-6} (α_C = 6.8 ppm/°C, α_S = 16.0 ppm/°C, $T_C = T_S$ = 100°C, $T_{C,0}$ = $T_{S,0}$ = 0°C), h = 0.005 in;

-> ΔD(test) = 1.030x10^{-2}.

and for the field use: F = 0.7, L_D = 0.080 in, $\Delta(\alpha\,\Delta T)$ = 148.0x10^{-6}//222.0x10^{-6} (α_C = 6.8 ppm/°C, α_S = 10.5 ppm/°C, $T_C = T_S$ = 85°C, $T_{C,0} = T_{S,0}$ = 45//25°C), h = 0.005 in;

-> ΔD(use) = 1.658x10^{-3}//2.486x10^{-3} at ΔT = 40//60°C, respectively.

The input parameters into Eq. A-2 are for the test: T_{SJ} = 50°C ($T_C = T_S$ = 100°C, $T_{C,0} = T_{S,0}$ = 0°C), t_D = 15 min;

-> c(test) = –0.4160;

and for the field use: T_{SJ} = 65//55°C ($T_C = T_{S,0}$ = 85°C, $T_{C,0} = T_{S,0}$ = 45//25°C), t_D = 715 min;

-> c(use) = –0.4739//–0.4679 at ΔT = 40//60°C, respectively.

Using these results into Eq. A-12 in IPC-SM-785 with N_f(test, 50%) = 10,612 cycles gives:

=> N_f(use, 50%) = 148,000//73,000 cycles at ΔT = 40//60°C, respectively.

Conclusions:
The two components analyzed have large reliability margins for this use environment; a product with 30 chip carriers and 100 CC1820s would just reach a cumulative failure probability of 0.5% after 10 years.

Excellent agreement between the reliability estimates from analytical reliability model and from extrapolation from the results of accelerated testing is shown.

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Appendix B
Design for Reliability (DfR) of Plated-Through Via (PTV) Structures

B-1.0 PLATED-THROUGH VIA (PTV) RELIABILITY ISSUES

Plated-through-holes (PTHs) serve to electrically connect different conductor layers in multilayer printed circuit boards (MLBs). In conventional interconnection technology employing through-mounted components, the PTHs also serve the function of providing a structure that accepts the component leads and to which these leads can securely be solder attached. This structure consisting of the copper PTH barrel containing a component lead and filled with solder provides a very robust, multiple-redundant electrical and mechanical connection between the component and the MLB.

The continuing drive towards higher functionality, higher density, and lower weight was brought about and made possible by the development of surface mounted technology. This reduced the purpose of the previously multi-functional PTHs to providing only the electrical interconnections between the MLB layers; the diameters of PTHs could also be reduced, since they no longer needed to be large enough for the component lead insertion operation. To distinguish the two types of PTHs, the PTHs without component leads are frequently referred to as 'PTH-vias' or PTVs. At the same time, the increased functionality and density of the components often brought about a need to increase the number of layers in MLBs, and thus to increase the MLB thickness.

The decreasing PTV diameters, particularly in combination with the increasing MLB thicknesses, make copper plating into the PTVs more difficult. This problem was first recognized during an IPC round robin study [Ref. B-7: 1], which led to a more detailed round robin study specifically focused on this issue [Ref. B-7: 2]. PTVs having a small diameter—less than ~0.5 mm—and/or a high aspect ratio of MLB thickness to drilled PTV diameter—more than 4—were found to require special treatment for adequate reliability.

During this study the material properties, processing parameters, and environmental test and use conditions important for the reliability of PTVs were identified. The results of these studies together with prior and subsequent work [Refs. B-7: 3-9] has been utilized to develop a practical methodology to aid in the DfR of PTVs, as well as to permit the assessment of the reliability of PTVs given the assembly and test procedures and the use environments in the field [Ref. B-7: 10].

In the IPC round robin test program [Ref. B-7: 1] the IEC (Hot Oil Test, IEC 362-2) test—designed to simulate solder reflow thermal shock cycles—was used to evaluate the reliability of small-diameter PTVs. It was found that assembly processes involving large temperature excursions constitute a significant reliability threat due to low-cycle fatigue for PTV copper barrels with low ductility or large stress concentrations. It was concluded that failures, to the extent they occur at all, occur typically in the first 10 cycles due to overstress crack initiation followed by crack propagation. This conclusion was reinforced by the findings of Oien [Refs. B-7: 3, 4], which showed that crack initiation typically occurs during the first or second cycle of overstress. Unless failure occurs within 10 cycles of the overstress loading typical of solder reflow, solder reflow overstressing is not a problem. Additional cycles will eventually lead to fatigue-induced failures. The failures that occurred in the IPC study were observed in product from vendors rated 'poor' to 'good' on an arbitrarily subjective scale with some consistency in differentiation. No superior-rated vendor product failed, but it has to be noted that the testing had an arbitrary cut-off. This led to the definition of a numerical quality index that is now utilized in an improved more detailed form in the reliability modeling shown in Reference B-7:2 [Ref. B-7: 10].

During the product use, the severity of the thermal use environment has a great impact on the reliability of the PTVs. The "MIL-T" and "COM-T" thermal cycling tests [Ref. B-7: 2] were designed to simulate severe and relatively benign use environments, respectively. While failures in the "MIL-T" test occurred depending on the construction of the MLBs and the quality of the PTVs, failures did not occur as the result of the "COM-T" test. It needs to be noted however, that the "MIL-T" and "COM-T" thermal cycling tests unfortunately had arbitrary test cut-offs at 400 and 1000 cycles, respectively.

B-1.1 Copper Plating Process

B-1.1.1 Acid Copper Plating One finding of the IPC round robin study [Ref. B-7: 2] was that PTVs with aspect ratios larger than three and plated with standard electrolytic acid copper show decreasing thermal cyclic fatigue life. It was found that the copper plating process window narrows as the PTV aspect ratio increases and that the standard electrolytic plating processes become inadequate even with optimum process controls. These findings agree with earlier studies investigating the effects of plating current density and agitation level on copper deposit quality in PTVs [Ref. B-7: 5]. In this study it was shown that inadequate electrolyte replacement rates, which can clearly occur in high-aspect-ratio PTVs, will lead to mass-transport limited

plating conditions. Under these conditions, in combination with the non-uniform plating current densities that also get worse with increasing aspect ratios, the copper deposit quality rapidly deteriorates with increasing aspect ratios. The resulting copper deposits within the PTV can have significantly lower ductility and strength than the copper deposits plated at the same time external to the PTVs, e.g. on plating mandrels. The decline in physical properties is frequently accompanied by increased 'dog-boning' and nodule formation as well [Ref. B-7: 10].

The copper deposits from standard acid copper baths in high-aspect-ratio PTVs, even with uniform plating in the PTV barrels and good intrinsic tensile properties, as determined by testing foil specimens from flat plating mandrels, perform only marginally in thermal cycling tests. For this reason, special plating solutions have been developed, that allow reduced plating current densities at the expense of increased plating times, but producing significantly improved PTV copper barrel reliability.

B-1.1.2 Pyrophosphate Copper Plating Pyrophosphate plated copper was unfortunately not part of the IPC round robin studies [Refs. B-7: 1, 2]. It has however been shown, that pyrophosphate copper is less susceptible to the effects of non-uniform plating current densities and higher PTV aspect ratios.

B-1.2 Material Properties

B-1.2.1 Tensile Properties The tensile properties of the PTV copper deposits are very important, both for the performance of the PTVs during subsequent processing and use, and for the DfR for the PTVs. The properties that are needed are: (1) the tensile strength, (2) the yield strength, (3) the modulus of elasticity, (4) the modulus of plasticity, and (5) the fracture ductility.

It has also been found, that the electrolytically plated copper deposits have a modulus of elasticity significantly below that of cast and rolled copper reported in material property references. It therefore is necessary to measure the modulus of elasticity, which can be done during the tests to determine the yield and tensile strengths of the deposits.

The tensile strength, the yield strength, the modulus of elasticity and the modulus of plasticity can be determined from tensile tests. To properly determine the modulus of elasticity, the 'interrupted tensile test' method should be utilized.

It needs to be noted however, that these tensile properties come from samples plated onto flat stainless steel mandrels and only set the upper bounds for the strength and ductility of the copper deposit inside the PTV. The evidence is circumstantial, but very strong, that these properties are significantly degraded inside of high-aspect-ratio (board thickness/PTV-diameter) PTVs [Ref. B-7: 2].

B-1.2.2 Ductility The tensile elongation is a very inaccurate and subjective test for foil samples because of the specimen geometry and the dependence on the test conditions [Ref. B-7: 10, 11]. Tensile elongation for foil materials is adequate for quality control and comparison purposes, but it significantly underestimates the fracture ductility of the material by about a factor of three (3) and gives the false indication of a ductility dependence on foil thickness.

It is for these reasons that the test cited in References B-7:12 and 13, was developed. This test has a high discrimination power in terms of quality variations of the copper deposit, thus being very valuable as a process control tool as well as providing direct input for the all-important ductility of the copper deposit.

In order to assess the quality of the plated copper deposits, foil samples plated onto mandrels need to be subjected to fatigue ductility testing [Ref. B-7: 12].

It needs to be noted however, that this ductility comes from samples plated onto flat stainless steel mandrels and only set the upper bounds for the ductility of the copper deposit inside the PTV. The evidence is circumstantial, but very strong, that this property is significantly degraded inside of high-aspect-ratio (board thickness/PTV-diameter) PTVs [Ref. B-7: 2].

The ductility of the copper deposit in the PTV barrel can be determined from the performance of the PTVs in accelerated testing resulting in low-cycle fatigue. In Table B-1 the results from two of the tests used in the Reference B-7:2 applied to coupons from the same sample are given together with the stresses and strain ranges resulting from the thermal cycling/shock excursions. Also given is the minimum ductility resulting from the first failures in the tests using Eq. #1 in Section B-2.0 together with the initial tensile strength.

The measured mandrel ductility was about 30%. Thus, the ductility in the PTV barrels as given in Table B-1 indicates a significantly lower deposit ductility as compared to the ductility of the deposit on the MLB surface.

B-1.2.3 Fatigue Behavior It has been found that annealed electrolytic acid copper strain-hardens upon the application of cyclic strain loads during fatigue tests [Ref. B-7: 11]. This results in high-cycle fatigue lives that are longer than expected based on the initial material properties.

Conversely, annealed pyro-phosphate-plated copper strain-softens as the result of the application of the cyclic strains during the fatigue testing. Therefore, fatigue life tests in the

Table B-1 Estimates of Tensile Properties of Copper Deposit Inside the PTVs [Reference B-7:10]

Test	ΔT [°C]	Fatigue Life N_f [cycles]	Barrel Stress σ [MPa/ksi]	Strain Range $\Delta\varepsilon_{max}$ (eff) [%]	Copper Strength S_u [MPa/ksi]	Minimum Ductility D_f [%]
IEC Hot Oil Thermal Shock	235	32	219/31.8	4.5	281/40.7	20.6
Temperature Cycle/Shock	190	150	177/25.7	2.2	281/40.7	23.3

high-cycle regime as per Reference B-7:12 need to be performed in order to obtain an indication of the changes in the material properties from either strain-hardening or softening during high-cycle fatigue. By using larger bend mandrel diameters than are used for the fatigue ductility test, the samples are subjected to high-cycle fatigue to assess the material behavior of the copper plating under extended fatigue loading.

B-1.3 Damage Mechanisms and Failure

B-1.3.1 PTV Quality The quality of the PTVs, together with the severity of the thermal expansion loading, is the critical aspect in the reliability of PTVs.

Even good quality PTVs will eventually fail and will typically do so as the result of a PTV barrel fracture near the center of the barrel as is illustrated in Fig. B-1.

PTV failures can also occur as the result of PTV shoulder fractures (see Fig. B-2) and internal land fractures. Failures of these types typically are the consequence of an inadequate material choice for the vendor copper foils [Ref. B-7: 14] used for the laminates or some processing error.

Of the ΔT≈180°C thermal excursion during the soldering process, ΔT≈100°C is below T_g at a mismatch in the

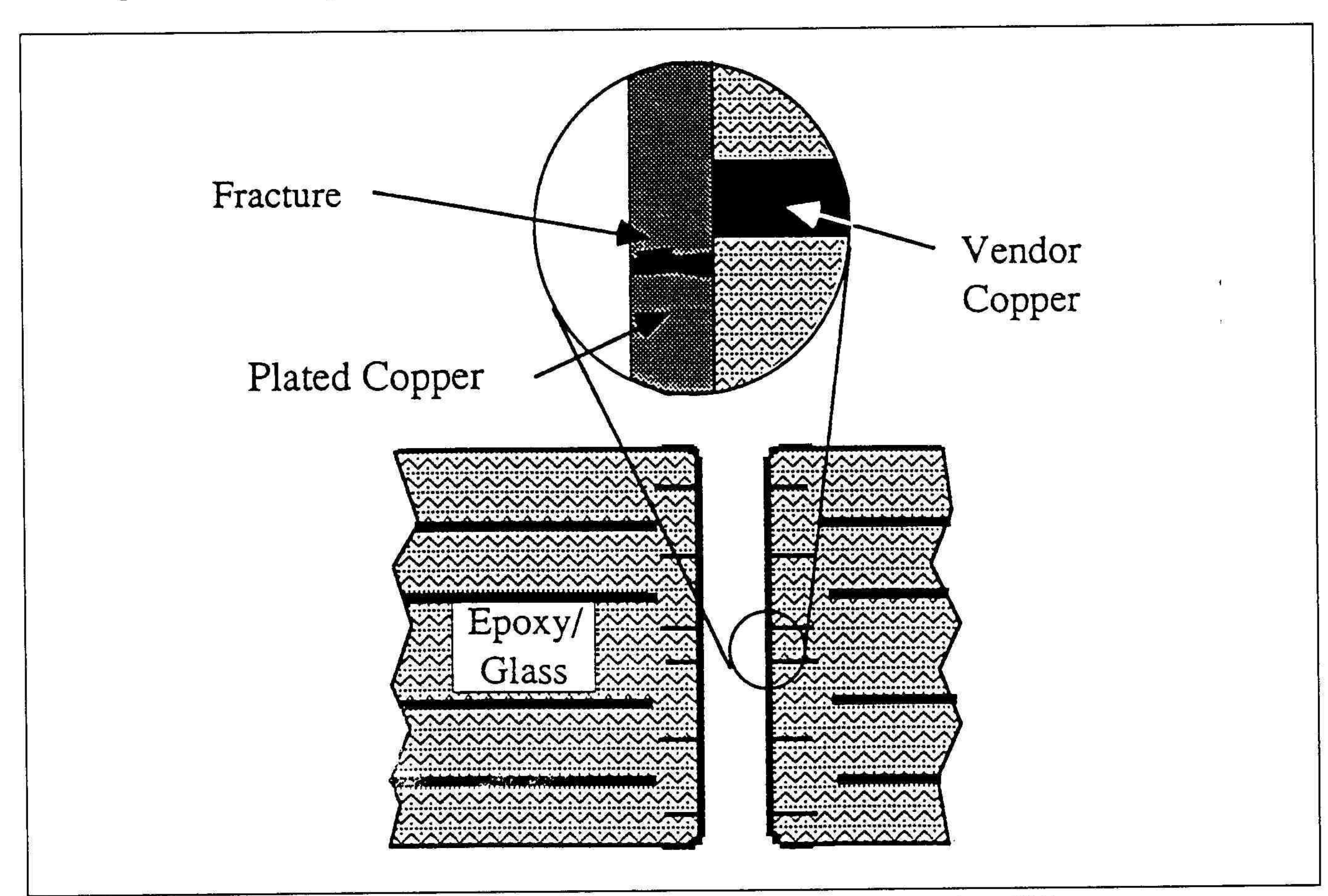


Figure B–1 Cross-Section Schematic of a PTV With a Barrel Fracture Near the Center of the MLB

CTEs of $\Delta\alpha \approx 20\text{-}69$ ppm/°C, whereas $\Delta T \approx 80°C$ is above T_g at a mismatch in the CTEs of $\Delta\alpha \approx 168\text{-}331$ ppm/°C. This results, for a 1.60 mm thick MLB, in an expansion mismatch between ~25 and 50 µm, providing the severe loading conditions that can lead to fractures in the PTV barrels or shoulders as well as the cracking of inner copper layers near the MLB surface.

The most typical failure mode, however, is the fracture of the PTV copper barrel, which is the primary subject here. is the resulting thermal expansion mismatch causing stresses in the PTV copper barrel and shoulders.

The large temperature excursions during the soldering and solder reflow processes combine with the difference in the CTE between the glass-reinforced epoxy layers surrounding the PTV and the plated copper of the PTV barrel to create tensile stresses in the copper barrel and bending stresses at the PTV shoulder due to the PTV land rotating as a result of the large z-direction (the direction perpendicular to the plane of the MLB) expansion of the epoxy. The CTE of FR-4 in the z-direction is typically 38-97 ppm/°C below the glass transition temperature, Tg, and 186-349 ppm/°C above T_g [Refs. B-7: 15-20], whereas electrodeposited copper foils have a CTE of about 17±2 ppm/°C.

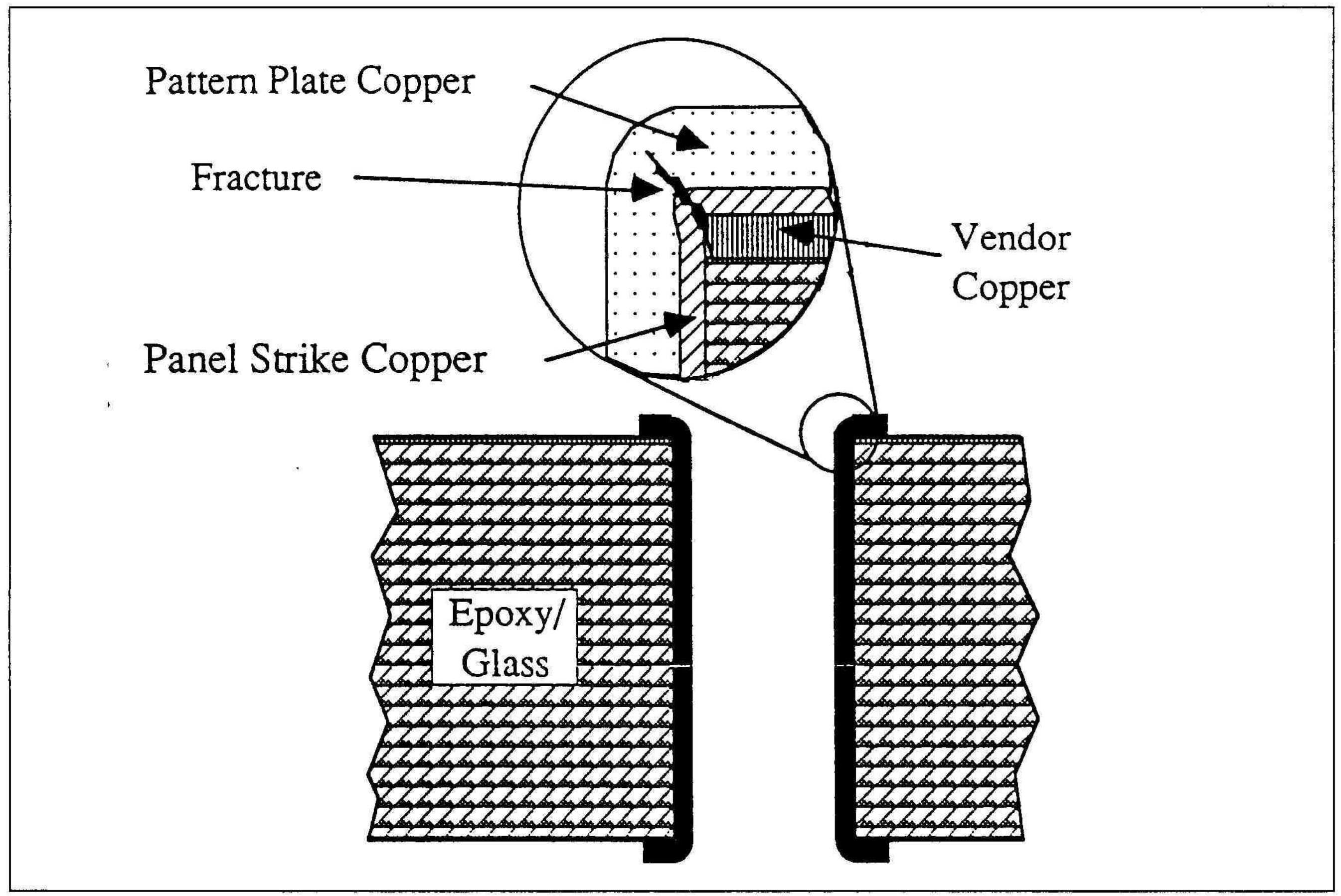


Figure B–2 Schematic Cross-Sectional View of a PTV with a Shoulder Fracture in a printed board

In Section B-2.0 on reliability modeling, an attempt is made to distinguish between three different quality aspects of PTVs. One of these is related to the quality of the PTV walls as the result of the drilling and desmear processes, and two to the plating quality in terms of the plating uniformity 'dog-boning' and the reduced material properties in the center of the PTV.

B-1.3.2 Impact of Assembly Processes and ESS Procedures The most severe stress condition and threat to reliability for PTVs takes place during the solder reflow processes necessary to make circuit board assemblies. Because of the large differences in the CTEs for the copper and the MLB resin, the larger the temperature excursions the larger

Environmental Stress Screening (ESS) procedures, in order to be effective, need to resemble solder reflow excursions in their severity. Therefore, ESS cycles have a similar impact as do solder reflow excursions.

It is during these excursions to solder reflow temperatures during solder reflow operations or ESS procedures that PTV barrel cracks can initiate due to overstressing and

subsequent thermal excursions serve to propagate such cracks to complete separation and failure.

B-1.3.3 Impact of Test Procedures and Cyclic Operating Environments During cyclic temperature testing and operational use of the product, cyclic thermal excursions can also lead to fractures and failure due to cyclically accumulating fatigue damage. The severity of the fatigue damage is dependent on the severity of the operational environment of the application. In Table A-1 guidelines as to the possible use environments for nine of the more common electronic applications are illustrated. The fatigue damage caused first by the thermal excursions during processing and assembly, then by cyclic temperature testing, and finally during product use is cumulative and needs to be accounted for in a reliability analysis.

B-2.0 RELIABILITY PREDICTION MODELING

The fatigue behavior of metals can be described by [Refs. B-7: 21, 22]

$$\overline{N_f}^{-0.6} D_f^{0.75} + 0.9 \frac{S_u}{E} \left[\frac{\exp(D_f)}{0.36} \right]^{0.1785 \log \frac{10^5}{\overline{N_f}}} - \Delta\varepsilon = 0 \quad \text{(Eq. B-1)}$$

where

$\overline{N_f}$ = mean fatigue life, cycles-to-failure,

D_f = fracture ductility, plastic strain at fracture, of the PTV copper deposit,

S_u = tensile strength of the PTV copper deposit,

E = modulus of elasticity of the PTV copper deposit,

$\Delta\varepsilon$ = total cyclic strain range.

The relationships underlying Equation B-1 were developed to be able to predict the fatigue life from tensile properties and brought about a unified ductility-dependent low-cycle fatigue and strength-dependent high-cycle fatigue [Ref. B-7: 23] approach. Equation B-1 has been used for some major study programs [Refs. B-7: 2, 11, 24] and the development of test methods [Refs. B-7: 12, 13].

The full determination of the stresses and strains in the PTV barrel requires a complex and expensive FEA [Refs. B-7: 7-10] which goes significantly beyond the needs for a reliability estimate. For the purposes of DfR and a reliability estimate, the stresses and strains can be estimated with adequate accuracy using a practical engineering approach [Ref. B-7: 10]. The closed form approach, given below, assumes no land rotation—a conservative assumption—and calculates the average stresses and strains assuming a uniform stress and strain distribution. This last assumption is non-conservative; corrections (see Eqs. B-11 through B-14), based on empirical test results, need to be applied. Depending on the magnitude of the PTV barrel deformation, the average stresses are calculated by

$$\sigma_{avg} = \frac{(\alpha_E - \alpha_{Cu})\Delta T A_E E_E E_{Cu}}{A_E E_E + A_{Cu} E_{Cu}}, \text{ for } \sigma_{avg} \le S_y \quad \text{(Eq. B-2)}$$

or

$$\sigma_{avg} = \frac{\left[(\alpha_E - \alpha_{Cu})\Delta T + S_y \frac{E_{Cu} - E_{Cu}'}{E_{Cu} E_{CU}'}\right] A_E E_E E_{Cu}'}{A_E E_E + A_{Cu} E_{Cu}'}, \text{ for } \sigma_{avg} > S_y \quad \text{(Eq. B-3)}$$

where

$$A_E = \frac{\pi}{4}\left[d_E^2 - d^2\right] \quad \text{(Eq. B-4)}$$

and

$$A_{Cu} = \frac{\pi}{4}\left[d^2 - (d-2t)^2\right] \quad \text{(Eq. B-5)}$$

and where

σ_{avg} = PTV barrel stress;

S_y = PTV barrel copper yield strength, typically ~172 MPa;

α_E = CTE of MLB in thickness direction, for excursions above T_g the larger CTE at those temperatures needs to be considered, typically ~65 ppm/°C @ <T_g, 315 ppm/°C @ >T_g;

α_{Cu} = CTE of copper, typically ~18 ppm/°C;

ΔT = temperature range of thermal cycling;

A_E = area of loading influence of MLB;

A_{Cu} = area of PTV barrel;

E_E = modulus of elasticity of epoxy, typically ~3.5 GPa;

E_{Cu} = modulus of elasticity of PTV copper, typically ~83 GPa for acid- plated copper and 35 ~GPa for pyrophosphate-plated copper;

E_{Cu}' = modulus of elasticity of PTV copper, typically ~0.7 GPa;

h = thickness of MLB;

d = drilled PTV diameter;

d_E = diameter of MLB dielectric surrounding the PTV and influencing the PTV loading;

t = thickness of copper deposit in PTV barrel.

The average strains in the PTV barrel are determined from

$$\Delta\varepsilon_{avg} = \frac{(\alpha_E - \alpha_{Cu})\Delta T A_E E_E}{A_E E_E + A_{Cu} E_{Cu}}, \text{ for } \sigma_{avg} \le S_y \quad \text{(Eq. B-6)}$$

and

$$\Delta\varepsilon_{avg} = \frac{(\alpha_E - \alpha_{Cu})\Delta T A_E E_E - S_y A_{Cu} \frac{E_{Cu} - E_{Cu}'}{E_{Cu}}}{A_E E_E + A_{Cu} E_{Cu}'}, \text{ for } \sigma_{avg} > S \quad \text{(Eq. B-7)}$$

where

$\Delta\varepsilon_{avg}$ = the cyclic strain range during thermal cycling.

The diameter of MLB dielectric material surrounding a PTV and influencing the PTV loading, d_E, is a measure of

the stiffness of the MLB structure surrounding the PTV barrel. The degree of land rotation—and thus lower stiffness—and any other stiffening structures, such as reinforcement weave, neighboring PTVs, components and cooling plates, will have an impact on this stiffness. For bare MLBs it was found that d_E could vary from a relatively small diameter of influence [Ref. B-7: 10]

$$d_E \cong 3d \qquad \text{(Eq. B-8)}$$

for softer structures to possibly a very large diameter of influence [Ref. B-7: 10]

$$d_E \cong 2h \qquad \text{(Eq. B-9)}$$

for PTVs in MLB assemblies for which land rotation is essentially prevented by large stiff components and heat sink plates; the most probable representative value for bare MLBs is [Ref. B-7: 10]

$$d_E \cong \frac{h}{2} + 2d \qquad \text{(Eq. B-10)}$$

It has been found [Refs. B-7: 2,7,10] that the average barrel strains, $\Delta\varepsilon_{avg}$, thus calculated need to undergo a correction for the assumptions necessary for a closed form stress and strain analyses. Further, stress concentrations can occur due to the uneven PTV barrel geometries resulting from inadequate drilling and/or plating processes. In addition, localized differences in the resin content (B-stage layers) and the influence of inner lands and power and ground planes can cause non-uniformities in the stresses and strains, and at temperatures above T_g, the material properties of the polymeric dielectric materials change dramatically and abruptly [Ref. B-7: 10].

Furthermore, PTV failures, as all failures due to wearout mechanisms, have a statistical distribution. The available data are not adequate to fully define this statistical distribution, but wearout mechanisms like fatigue typically follow a Weibull distribution with a shape parameter or slope of $\beta \approx 3$. Typical data are reported as the first failure from a number of daisy chains with upwards of 100 PTVs each.

An effective maximum strain range to be used in Eq. B-1 can be found from

$$\Delta\varepsilon_{max}(\text{eff}) = K_{eff}\,\Delta\varepsilon_{avg} \qquad \text{(Eq. B-11)}$$

where K_{eff}, the effective PTV strain coefficient, results from a combination of discernible deviations from a uniform stress and strain distribution, such that

$$K_{eff} = K_d\,K_b\,\frac{100}{K_c}\,\frac{10}{K_Q} \qquad \text{(Eq. B-12)}$$

The coefficients in Eq. B-12 are the PTV strain distribution factor, K_d, the plating thickness 'dog-boning' coefficient, K_b, the PTV stress concentration factor, K_c, and the PTV plating quality index, K_Q. Initially, the last three coefficients had been combined in a general PTV quality index [Ref. B-7: 2], but by separating the discernible quality variations, the source of the reduced quality can be identified and the impact less arbitrarily quantified. As a guideline it should be noted that the values for K_{eff} in Reference B-7:2 varied between about 1.2 and 10.

The PTV strain distribution factor, K_d, corrects for the model assumption of a uniform stress and strain distribution for a distribution that is in fact non-uniform. The non-uniformity is a function of the MLB thickness, h, with higher non-uniformities resulting from thicker MLBs. The PTV strain distribution factor is also dependent on whether or not the temperature excursions exceed T_g, above which not only the thermal expansion increases, but the materials softens significantly. Thus

$$K_d = \begin{cases} 1 & , T_{max} > 200°\text{C, any } T_g \\ 1+1.5\left(\dfrac{h}{2.3\text{ mm}}\right)^3 \dfrac{T_{max} - T_g}{200 - T_g} & , T_{max} > T_g, \\ 1+1.5\left(\dfrac{h}{2.3\text{ mm}}\right)^3 & , \text{otherwise} \end{cases} \qquad \text{(Eq. B-13)}$$

The plating thickness 'dog-boning' coefficient, K_b, accounts for any non-uniform stress and strain distribution in the PTV barrel due to the gradual thinning—'dog-boning'—of the copper deposit towards the barrel center. This 'dog-boning' can result from plating conditions that are slightly beyond the capability of the plating chemistry used. The coefficient is given by [Ref. B-7: 10]

$$K_b = \frac{t_{PTV\ shoulder}}{t_{PTV\ center}}$$

The PTV stress concentration factor, K_c, is a measure of the stress concentrations caused by the localized abrupt thinning of the copper deposit due to either drilling or plating defects. Its size may be taken from Figure B-3 using the plating deposit narrowing to determine the local 'reduction in cross-section'.

Figure B-3 contains a curve [Ref. B-7: 10] which quantifies the large impact stress concentrations due to localized thinning of plated copper conductors on flexible printed wiring have on increasing the stress—and thus the strain—locally. PTV copper barrels, however, due to their three-dimensional geometric structure are less susceptible to stress concentrations that occur as localized features visible on two-dimensional cross-sections. Figure B-3 also contains a curve which is an attempt to quantify the impact of these localized stress concentrations, which do not affect the whole PTV barrel cross-section, in terms of the portion of the basic material ductility that is required to accommodate these stress concentrations. From Figure B-3 a localized reduction in plating thickness by 50% would result in a value for K_c of about 82, raising the effective strain due to the stress concentration by about a factor of 1.22.

The PTV plating quality index, K_Q, is on a 10-to-1 scale

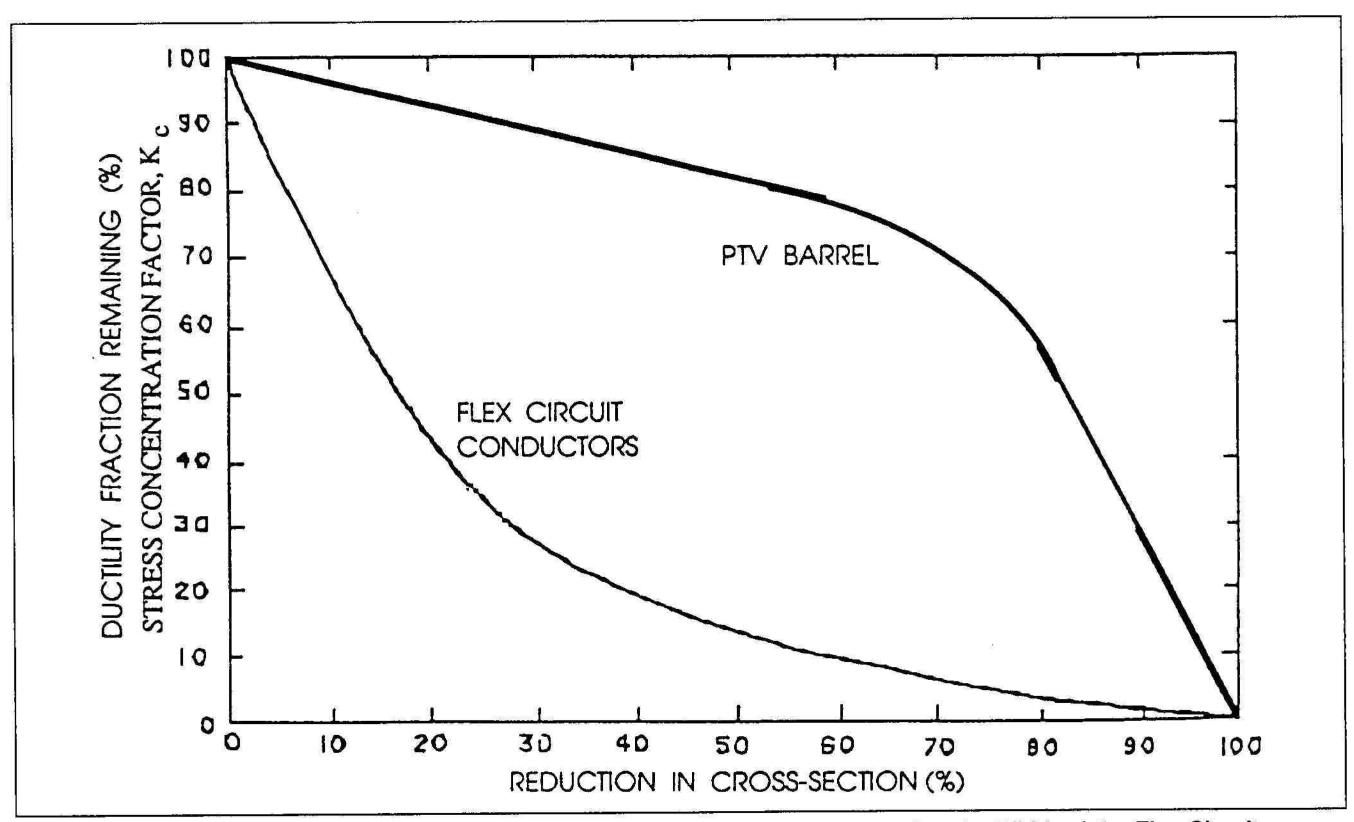


Figure B-3 Reduction of Available Copper Ductility Due to Localized Nicks Reducing the Width of the Flex Circuit Conductors [Ref. B-7: 25] and PTV Stress Concentration Factor, K_c.

with 10 being perfect, and is a measure of the quality of the plated copper deposit in terms of its material properties relative to those of a corresponding foil sample plated onto a plating mandrel. This index needs to be established by experience with PTVs in coupons or MLBs fatigued to failure.

B-3.0 DfR-PROCESS

A successful 'Design for Reliability'-process requires that a number of issues be addressed at the design stage. The generally applicable guidelines for the DfR-process are;

1) Keep PTV diameters as large as possible and the MLB thickness/PTV diameter aspect ratio as small as possible;
2) Require a nominal copper deposit thickness of 30 μm to obtain actual plating thicknesses in the range of 25 to 40 μm;
3) Use E3 copper foil for the signal, power, and ground layers for aspect ratios larger than 3:1;
4) Tent PTVs for applications with severe operational loading conditions (see Table B-2) with solder mask to prevent solder from partially filling the PTVs and causing stress concentrations.

It is much more difficult to plate consistent high quality copper deposits into small-diameter PTVs using standard electrolytic processes. Also, smaller diameter PTV barrels, especially in thicker MLBs, are subjected to higher loading conditions.

A plating thickness of ~25 μm has been found to be the minimum thickness which gives good reliability; a plating thickness of ~40 μm is optimum from a reliability perspective. Plating thicknesses greater than that tend to promote shoulder fractures (see Fig. B-2).

The quality of the copper foil for the signal, power, and ground layers is of importance for aspect ratios larger than about 3:1. Standard E1 copper foil [Ref. B-7: 14] has a coarse columnar grain structure with the grain boundaries perpendicular to the foil surfaces and has an elongation requirement of only 2%. Thus, brittle E1 vendor foil can lead to signal layer fractures and shoulder cracks as illustrated in Figure B-2. 'High Temperature Elongation' -E3 copper foil is recommended for PTVs with aspect ratios larger than about 3:1.

Tenting the PTVs is a prudent and pragmatic decision. PTVs entirely filled with solder certainly are more robust and reliable than PTVs without solder; the problem is that it cannot be guaranteed, that all the PTVs will be entirely filled with solder. Partially solder-filled PTVs have stress concentrations where the transition from fully filled to partially filled occurs; these stress concentrations reduce the

reliability of these PTVs significantly. Therefore, it is best to avoid the possibility of these stress concentrations all together by tenting the PTVs. However, it needs to be emphasized, that this issue is important only for severe use conditions with temperature cycles of about ΔT≥50°C, as can be seen in Table B-2.

In Table B-1 in Section B-1.2.2 the minimum fatigue ductilities resulting from two accelerated fatigue tests of PTVs in MLBs are given. These estimates of the copper deposit properties in the PTV barrels are used in Table B-2 to estimate the minimum fatigue lives for a number of typical electronic use environments. The fatigue lives are given together with the pertinent information on the use conditions and the resulting stresses and strains.

The results in Table B-2 indicate that the PTVs of good quality do not constitute a reliability threat to most product applications in the field. Only for the more severe use environments would premature failures be anticipated. However, the results in Table B-2 would change drastically for PTVs of low quality.

B-4.0 CRITICAL FACTORS FOR EMERGING ADVANCED TECHNOLOGIES

The emerging advanced technologies are characterized by denser packaging resulting in ever smaller structures. Thus, the temptation exists to drive the PTV diameters ever smaller and the aspect ratios higher. The DfR principles detailed in Section B-3.0 need to be kept in mind in the design and application of these emerging technologies.

B-5.0 VALIDATION AND QUALIFICATION TESTS

Validation and qualification tests have not been established for PTVs. However, the test procedures used in the IPC round robin program reported in IPC-TR-579, Round Robin Reliability Evaluation of Small Diameter Plated Through Holes in Printed Wiring Boards [Ref. B-7: 2], could be utilized for this purpose.

Efforts are underway within the IPC via a round robin test program to establish both qualitative and quantitative correlation for a number of promising test methods.

Table B–2 Estimates of the Fatigue Life and Time to Failure of PTVs in Some Typical Use Environments from Table A-1

Used Environment	ΔT [°C]	Estimated Maximum Annual Cycles	Barrel Stress σ [MPa/ksi]	Strain Range Δε [%]	Effective Strain Range $\Delta\varepsilon_{max}$(eff) [%]	Minimum Fatigue Life [cycles]	Estimated Time to First Failure [years]
Computers	20	1460	67/9.7	0.08	0.20	$8.0X10^6$	5 500
Telecomm	35	365	117/16.9	0.14	0.35	75 000	205
Industrial	60	250	173/25.1	0.28	0.71	2 900	12
Automotive	80	365	174/25.2	0.38	0.95	1 200	3.3

The DfR-process needs to emphasize a physics-of-failure approach. The process might involve the following steps:

A. Identify Reliability Requirements—
expected design life and acceptable cumulative failure probability at the end of this design life;

B. Identify Loading Conditions—
use environments (e.g., IPC-SM-785) and thermal gradients due to power dissipation;

C. Identify/Select Assembly Architecture—
substrate selections, material properties (e.g., CTE), PTV diameter, aspect ratio;

D. Assess Reliability—
determine reliability potential of the designed assembly and compare to the reliability requirements using the approach shown here; this process may be iterative;

E. Balance Performance, Cost and Reliability Requirements.

B-6.0 SCREENING PROCEDURES

The crucial task is the elimination of the MLBs with thin-plated PTVs without significantly affecting the remainder of the MLBs. The fact that the defects not only involve very thin plating (<10 μm), but occur in conjunction with substantial stress/strain concentrations, makes this task possible.

An Environmental Stress Screening (ESS) could employ the same test setup as the Hot Oil Test (IEC Specification 362-2, Test C) [Ref. B-7: 2], for three (3) to five (5) cycles. Thus, together with the solder reflow operations necessary for production, the MLBs would experience between eight (8) to ten (10) such temperature excursions.

Given the result, based on standard IEC test criteria, that the life under these loading conditions is 32 cycles, this would consume between 25 and 30 % of the MLBs lives. Considering the results in Table B-2, that still would leave adequate life for most use environments.

B-7.0 REFERENCES

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Appendix C
Design for Reliability (DfR) of Insulation Resistance

C-1.0 INSULATION RESISTANCE DAMAGE MECHANISMS AND FAILURE

The damage mechanisms work generally in two distinct regions: at the surface and in the bulk of the electronic assemblies, particularly the printed board. It has been reported, that surface and bulk phenomena exhibit different time constants in the response to temperature changes [Ref. C-7: 1]. The insulation resistance for a sample circuit is the measured integrated effect of both surface and volume resistivity as defined by ASTM [Ref. C-7: 2]. The measured bulk resistance will depend upon the nature of the laminate, solder mask and/or conformal coating under investigation. It will also depend upon the degree of cure of the polymers and for printed boards on the quality of the drilling process for the plated-through holes (PTHs) and vias (PTVs), and will be affected by soldering flux/paste residues if they dissolve into the polymeric material during the soldering and/or cleaning processes.

Insulation resistance measurements provide important data in the characterization of printed board laminates, multilayer boards (MLBs), soldering fluxes, solder masks, and conformal coatings. Such measurements have been used to study the effect of aging at accelerated conditions (temperature, humidity and/or bias voltage) to determine any detrimental effects on the reliability of the product.

Ohm's law states that the magnitude of the current, I, flowing through a circuit with a given resistance, R, is a linear function of the applied voltage, V, such that

$$V = IR \qquad \text{(Eq. C-1)}$$

The resistance is an extrinsic property of the material sample dependent on the resistivity of the material and the geometry of the sample. The resistivity, ρ, of a material is an intrinsic material property. The resistivity is determined from the length, l, of the sample and its cross-sectional area, A, and is related to R by

$$\rho = R\frac{A}{l} \qquad \text{(Eq. C-2)}$$

Resistivity that measures the resistance to current flow through the bulk of a sample it termed volume resistivity, ρ_v,

$$\rho_v = R\frac{A}{t} \qquad \text{(Eq. C-3)}$$

where t = the thickness of the bulk sample.

Surface resistivity, ρ_s, measures the ability of an insulator to resist the flow of current on its surface, such that

$$\rho_s = R\frac{A_s}{l} \qquad \text{(Eq. C-4)}$$

where A_s = the surface area and l is the length of the insulating strip.

C-1.1 Surface Insulation Resistance (SIR) Surface insulation resistance (SIR) measurements will depend on the nature of the surface contamination and the amount of moisture present during the measurement. Although SIR readings are a combination of both bulk and surface resistance, 99.9 % of the current leakage for FR-4 epoxy/glass laminate will occur on the surface of the laminate, since the ratio of the surface resistivity to the volume resistivity is 1:1000 [Ref. C-7: 3]. Test patterns for measuring volume resistance will either use electrodes on the top and bottom of the substrate (for z-axis measurements) or PTVs to PTV-patterns for measuring the x, y-resistance. SIR patterns are typically interdigitated comb patterns such as the IPC-B-24 coupon.

Some materials, notably polyglycol, act to reduce insulation resistance by absorbing water and/or forming a monolayer of water at lower than saturation humidity, e.g. 75% RH [Ref. C-7:4]

C-1.2 Electrochemical Corrosion Electrochemical corrosion of metallic conductors and the migration of metal ions between anode and cathode on a printed board can lead to circuit failure. It is important to understand the cause of these failures in order to select materials and processes for printed board manufacture, soldering, and cleaning which will minimize the occurrence of these failures. The tendency of the metal conductor to migrate under a bias voltage in humid conditions has been shown to decrease across the following series of metals [Ref. C-7: 5]

$$\text{Ag} > \text{Pb} > \text{Solder} > \text{Cu} \qquad \text{(Eq. C-5)}$$

Those metals whose hydroxides are more soluble at pH 7-9 have a higher migration rate. This is related to the pH gradient between the anode and cathode when a film of moisture is present.

In the case of SIR testing, the cathode is connected to the high voltage source while the anode is connected to ground. For electrochemical migration to occur, the pathway must exist for ions to move from the anode to the cathode. In the presence of moisture, the following electrochemical reactions can occur at the anode

$$\begin{aligned} H_2O &\rightarrow \tfrac{1}{2}O_2 + 2e^- \\ Cu &\rightarrow Cu^{+1} + e^- \\ Cu &\rightarrow Cu^{+2} + 2e^- \\ Pb &\rightarrow Pb^{+2} + 2e^- \\ Sn &\rightarrow Sn^{+2} + 2e^- \\ Sn &\rightarrow Sn^{+4} + 4e^- \end{aligned} \qquad \text{(Eq. C-6)}$$

The preferred species in the case of copper will depend on the anion that is present. In water Cu^{+2} is the preferred species except when Cl^- is present. In this case the formation of the $CuCl^{2-}$ will favor the formation of Cu^+ rather than Cu^{+2} [Ref. C-7: 6].

At the cathode the possible reactions are

$$\begin{aligned} \tfrac{1}{2}O_2+H_2O+2e^- &\rightarrow 2OH^- \\ 2H_2O+2e^- &\rightarrow 2OH^-+H_2 \\ Cu^{+2}+2e^- &\rightarrow Cu \\ Pb^{+2}+2e^- &\rightarrow Pb \\ Sn^{+2}+2e^- &\rightarrow Sn \end{aligned} \qquad \text{(Eq. C-7)}$$

C-1.3 Dendrite Growth In normal electrochemical dendritic growth, electrolytic dissolution of the metals occurs at the anode and reduction of the metal ions by plating out occurs at the cathode. Typical dendrites associated with a solder-coated copper comb pattern will be lead-needles with some tin. These appear as "tree-like" dendrites which begin at the cathode. As these surface dendrites grow, their effect on the total SIR reading is minimal until they are very close to the anode. At the point of bridging, the dendrite will burn out quickly due to the high current density. For this reason, the presence of dendrites is not easily determined by the electrical SIR readings. These readings are not taken frequently enough to insure that a measurement will be taken exactly when the dendrite bridges. Thus, it is customary to examine SIR samples under the microscope with back lighting after the test is terminated to visually observe if dendrites have formed.

C-1.4 Conductive Anodic Filaments (CAF) In the late 1970 's a new electrochemical migration failure mechanism was reported by Bell Laboratories [Ref. C-7: 6]. During the study of potential failure modes associated with high voltage switching applications, the subsurface formation of conductive filaments along the glass/epoxy interface was observed at high humidity conditions under application of a high (200-500 V) voltage. This conductive anodic filament (CAF) formation involved the dissolution of copper at the anode and the formation of a copper-containing conductive filament along the glass/epoxy interface. It was reported that these CAF contain copper associated with chlorine or sulfur [Ref. C-7: 8]; these contaminants are associated with the board manufacturing process. Others have observed only chloride- or bromide-containing copper filaments [Ref. C-7: 9]. It has been suggested that moisture causes hydrolysis at the glass/epoxy interface [Ref. C-7: 7]. It is postulated that the absorption of moisture by the epoxy causes swelling which can lead to a debonding between the epoxy and the glass fiber [Ref. C-7: 10]. This moisture-induced debonding can be accelerated with damage to the bond between the glass fibers and the surrounding epoxy during the drilling process [Ref. C-7: 11]. A capillary of moisture at these damaged interfaces is available for the electrochemical reactions described in Eqs. C-6 and C-7 when a bias voltage is applied.

C-2.0 INSULATION RESISTANCE MODELING

In order to make predictions as to the behavior and reliability of electronic assemblies in environments with varying levels of temperature and humidity, data from representative accelerated high stress tests are used to extrapolate to milder operating conditions. This extrapolation requires an appropriate valid extrapolation model. It is not a simple task to obtain either good accelerated test data or appropriate extrapolation models. [Ref. C-7: 12].

C-2.1 Insulation Resistance Degradation SIR measurements are a relatively quick way to evaluate the interaction of processing materials with a given substrate. Reliability assessment, however, requires significantly more effort. Assumptions must be made about the relationship of the operating and use environments to the accelerating test conditions with elevated temperatures, humidities, and bias voltages chosen to accelerate the rate of degradation by known mechanisms without introducing extraneous damage mechanisms. If the assumptions are correct, extrapolation of the results from the accelerated tests back to operating conditions will provide an estimate of the product reliability.

To accomplish this task, a statistically significant number of samples must be processed and tested to failure at different accelerated test conditions. The effect of the temperature on the rate of failure follows for these processes an Arrhenius relationship [Ref. C-7: 13]

$$k_T = k_0 \exp\left(\frac{-E_a}{kT}\right) \qquad \text{(Eq. C-8)}$$

where
- k_T = the reaction rate at a given temperature,
- T = absolute (Kelvin) temperature,
- k_0 = a constant,
- E_a = the activation energy of the reaction, and
- k = Boltzmann's constant.

The effect of relative humidity can be described by

$$k_H = k_0^1 \exp C(RH)^b \qquad \text{(Eq. C-9)}$$

where
- k_H = the reaction rate at a given relative humidity,
- k_0^1 = a constant,
- C = described as a constant but is likely temperature dependent (see Eq. C-10), and
- b = an exponent empirically observed in the range from 1 [Refs. C-7: 1,8] to 2 [Ref. C-7: 14].

For tests with a bias voltage of 52 V, the insulation resistance, IR, was found to have the following dependence on temperature and humidity [Ref. C-7:1]

$$\ln IR = \ln IR_{\infty} + \frac{E_T}{kT} - \frac{RH}{100}\frac{E'_{RH}}{kT}\,\mathrm{epx}\left[\frac{E''_{RH}}{kT}\right]$$

$$= \ln 3.7\mathrm{x}10^{-29} + \frac{2.51}{kT} - \frac{RH}{100}\frac{0.31}{kT}\exp\left[\frac{0.12}{kT}\right]$$

(Eq. C-10)

where

IR_{∞} = an empirical constant interpreted as the insulation resistance of the test sample at infinite temperature and zero humidity,

E_T = the activation energy for the temperature dependence, and

E'_{RH}, E''_{RH} = activation energies for the humidity dependence in eV

k = $8.62\mathrm{x}10^{-5}$ eV/°K

The form of Eq. C-10 is the consequence of the fact that the driving parameter, the vapor pressure of water, p_v, is dependent on temperature. The relationship of the vapor pressure of water with RH can be approximated in the temperature range from 0 to 75°C by

$$p_v = \frac{RH}{100}\exp\left[16.82 - \frac{5250}{T[K]}\right] \quad \text{(Eq. C-11)}$$

Under the assumption that the effects of temperature and humidity are independent of each other and that the relationships can be validly extrapolated, the expected life can be calculated from results of the accelerated tests using an acceleration factor, A.F., using

$$A.F. = \exp\left[\frac{E_a}{k}\left(\frac{1}{T_{life}} - \frac{1}{T_{test}}\right) - C(RH^b_{life} - RH^b_{test})\right]$$

(Eq. C-12)

where the subscript 'life' refers to the normal operating conditions and the subscript 'test' to the accelerated test conditions.

The failure mechanism is highly temperature dependent with activation energies, E_a, variably reported as a very low 0.02 eV for some samples below 60°C and 0.6 to 2.5 eV for all samples above 60-65°C [Ref. C-7: 15], 0.6 eV [Ref. C-7: 14], 0.9 eV [Ref. C-7: 8] and 2.51 eV [Ref. C-7: 1].

The value of C associated with humidity can be taken from Eq. C-10 with b=l; for b=2 and RH expressed in percent C has been reported as $4.4\mathrm{x}10^{-4}$ [Ref. C-7: 14].

C.2.2 Conductive Anodic Filament Failure The determination of the mean-time-to-failure (MTTF) for the CAF failure mode is more complicated.

The CAF-MTTF is not only dependent temperature, humidity, and bias voltage, but also on the PCB materials [Refs. C-7: 8,16], and the quality of the manufacturing processes, particularly drilling [Ref. C-7: 11].

Further, preconditioning in terms of both thermal shock [Ref. C-7: 17] and exposure to high humidity [Refs. C-7: 11,17] has been observed to reduce CAF-MTTF. There appears to be a two-step process in which pre-conditioning at an accelerated relative humidity will reduce the time for CAF failure to occur once voltage is applied. (1) Moisture absorption by the substrate leads to interfacial degradation at the glass/epoxy interfaces. This interfacial degradation can also be enhanced by prior thermal cycling, thermal shock or, by mechanical stresses. (2) Electro-chemical corrosion and oxidation of Cu to Cu^{n+} creates the ions which migrate under a bias voltage. The time to failure can be expressed as the sum of these two steps

$$t_F = t_1 + t_2 \quad \text{(Eq. C-13)}$$

Studies where the application of the bias voltage was delayed indicate that $t_1 \gg t_2$ [Ref. C-7: 10].

There is evidence of a threshold relative humidity below which this degradation mode will not be observed. It has been proposed that for a given voltage, V, and a temperature T, the relative humidity, in percent, corresponding to a constant failure probability is [Ref. C-7: 7]

$$RH = \left[\frac{2.3975 + \ln(c) + \frac{0.9}{kT} - 1.52\ln(V)}{5.47}\right]$$

(Eq. C-14)

where

c = $6.9\mathrm{x}10^{-4}$ for a failure probability of 0.5%.

C-3.0 DfR-PROCESS

For insulation resistance, DfR should perhaps stand for 'Design for Robustness' rather than 'Design for Reliability,' because reliability assurance implies some numerical certitude which is not attainable in this context.

Thus, a successful DfR-process is one that assures the highest level of robustness that is practically and economically achievable. This requires that a number of issues be addressed at the design stage. The generally applicable guidelines to maximize robustness are:

1) Keep conductor lines and spaces on the printed board as wide as possible;
2) Provide a controlled operating environment;
3) Conformally coat electronic product if it is subject to temperature fluctuations such that condensation can occur (the degree of protection will depend on both the type and method of application of the coating);
4) Provide a controlled storage environment;
5) Avoid water-soluble fluxes and fusing fluids containing polyglycols for high humidity operating environments and high DC voltage gradients, since some of these fluxes have been implicated in enhanced CAF formation;
6) Utilize CAF-resistant PCB materials for assemblies with high humidity operating environments and high

DC voltage gradients, since electronic circuitry is most prone to CAF formation under these conditions;

7) Avoid testing conditions which create failure mechanisms and failure modes which will not be observed during normal operating life and use conditions.

C-4.0 CRITICAL FACTORS FOR EMERGING ADVANCED TECHNOLOGIES

The emerging advanced technologies are characterized by denser packaging resulting in ever finer conductor line widths and spacings. Without changes in the material and the operating environment, which for economical and practical reasons are not likely, finer lines and spacings result in reduced insulation resistance and increased threat of CAF formation. The DfR principles listed in Section C-3.0 need to be kept in mind in the design and application of these emerging technologies.

C-5.0 VALIDATION AND QUALIFICATION TESTS

C-5.1 SIR Test Procedures The most commonly used test vehicle for measuring SIR is an interdigitated comb pattern. These patterns exist in a variety of configurations with spacing between conductors ranging from 0.15 mm to 1.25 mm. SIR tests are carried out at elevated temperature and humidity levels; however, some tests are performed with a bias voltage applied throughout the duration of the test, while others are performed without electrical bias being applied.

Bias voltages applied during testing ranges from 10 V to as much as 500 V. Periodically a test voltage of typically 100 V, for the electrically biased tests with reversed polarity, is applied to measure the insulation resistance. In the case of the electrochemical migration tests required by Bellcore [Ref. C-7: 18] the bias voltage and the test voltage have the same polarity.

SIR tests are normally performed at accelerated conditions with elevated temperature and humidity levels. The test conditions range from 35°C/95%RH to 85°C/85%RH with test durations varying from 100 to 500 hours. Pass criteria also vary from 100 MΩ to 200 MΩ. The electrochemical migration test requires that any decline in insulation resistance be less than a decade for the sample to pass. Table C-1 compares the variation in the test conditions for the IPC SIR test [Ref. C-7: 19] for soldering flux and the Bellcore SIR and migration tests [Ref. C-7: 14].

The variation in the test parameters, as illustrated in Table C-1, results in a large variation in observed SIR data. As indicated previously, the insulation resistance is an extrinsic property of the material sample under investigation. This property will be affected by the test pattern, temperature, humidity, bias voltage and duration chosen for the test as well as the contamination associated with prior processing steps. This contamination may result in electrochemical corrosion.

SIR readings are sensitive to and affected by a number of factors.

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C-5.1.1 Factors Affecting SIR Readings

Geometry The geometry of the test pattern is of primary importance. When a bias voltage is applied, an interdigitated comb pattern experiences a distributed resistance due to the number of parallel traces over which the measurement is taken. The length of the interacting conductors divided by the separation between conductors is defined as the number of squares. In comparing data from two different comb patterns, the readings are sometimes reported as ohms/square.

Humidity When a monolayer of water is absorbed onto the surface of an epoxy/glass printed board, the water molecules hydrogen-bond to the epoxy making them essentially immobile. These hydrogen-bonded water molecules can exist as either continuous coatings or as discrete islands [Ref. C-7: 20]. As subsequent water layers are added, thicker films are formed allowing the dissolution of contaminants and the formation of hydrated ions which can move under the influence of an electric field [Ref. C-7: 21]. Conductivity measurements made on aluminum oxide revealed that for films with thicknesses of less than three (3) monolayers, the surface conductivity is two orders of magnitude below that of bulk water [Ref. C-7: 22]. The surface conductivity increased asymptotically with the increase in the number of monolayers with equilibrium being reached above 20 monolayers. Evidence indicates that there is a critical relative humidity at which a compound exhibits a surge in moisture absorption [Ref. C-7: 23,24]. For example, it has been demonstrated that dendritic growth of gold on alumina surface is dependent upon the relative humidity and that there existed a threshold for gold migration to occur [Ref. C-7: 25]. It has been shown, that the critical relative humidity for epoxy coatings is 70% and that the epoxy degrades over time when exposed to humid environments [Ref. C-7: 26].

Table C–1 SIR Test Parameters for Some Industry Tests

Parameters	IPC-TM-650 Solder Flux	Bellcore SIR	Bellcore Electromigration
Test Voltage	100 V	100 V	45 to 100V
Bias Voltage	50 V	50 V	10 V
Polarity	Reverse	Reverse	Same
Environment	85°C/85%RH	35°C/85%RH	85°C/85%RH
Duration	7 days	4 days	500 hours
Lines/Spacing	0.4/0.5 mm	0.64/1.27 mm 0.32/0.32 mm	0.32/0.32 mm
Number of Squares	~1000	~100 ~500	~500
Failure Criteria	100 MΩ	10^5 MΩ $2x10^4$ MΩ	SIR less than 1 decade decline

Contamination The presence of contamination on the surface will increase the moisture absorption. The critical relative humidity can be lowered by the presence of contaminants. The nature of these contaminants will determine how much moisture is absorbed at a given humidity level. If these contaminants are ionic in nature, they can enhance electrochemical reactions that occur in the presence of a bias voltage.

Voltage The bias voltage applied across the insulator will set-up a response in the dipolar polymer substrate. In performing SIR testing, it is important that the bias voltage chosen is realistic as it relates to the actual operating and use conditions of the electronic assembly. Typical test methods require 45-50 V bias because this represents a moderate accelerating condition relative to the +/- 15 V circuits common in telecommunication hardware. Excessively high voltage tests for routine circuits can lead to damage mechanisms and failure not representative of product use.

C-6.0 SCREENING PROCEDURES

For the threats to reliability from low SIR and CAF formation no effective screening procedure exists. The best that can be done is following the DfR recommendations in Section C-3.0 and the testing of representative samples using the test procedures discussed in Section C-5.0.

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Appendix D
Thermal Considerations

D-1.0 GENERAL

The designer of an SM PWA will be constrained by several external thermal factors:

A. The preference for cost and noise reasons is to cool by free convection or by conduction of heat to the outside atmosphere through thermally conducting copper planes, metallic cardguides and thermally conducting structural ribs in the system chassis.

B. The preference for contamination and corrosion control is to seal the PWA away from external air.

C. The heat densities and hotspot temperatures may require active (forced) cooling with media such as air or heat control fluids moved by fans or pumps.

D. The spacing between PWAs, the component spacings and geometries, as well as air velocities may result in either laminar or turbulent flows, affecting both heat removal from heat dissipaters and heat transfer to thermally sensitive components.

The primary thermal parameter which the designer must address is the temperature of the junction or active film of the component; both the absolute maximum or peak temperature and the steady state operating temperature limits imposed by the component manufacturer (as modified by derating protocols) must be observed. The secondary thermal parameter is the solder joint temperature since large temperature swings in service will subject the joint to conditions leading to cyclic fatigue, and long service times at high temperatures will grow copper-tin intermetallic compounds. See also IPC-SM-785, IPC-D-275, and IPC-SM-782.

For near-eutectic tin/lead solders - the most commonly used solders for surface mounted assemblies - good engineering practices result in typical operating temperatures of about 70°C. Higher levels of temperature are associated with faster aging of the solder joints due to metallurgical changes of the material structure and composition. Cyclic variations of the joint temperature are associated with fatigue degradation, solder being the compliant part of the system which has to accommodate relatively large differential expansions of the different materials. The fatigue life of the system is dictated primarily by the temperature swing, dwell time and lead compliancy and it is less dependent on the absolute value of temperature and the rise time necessary to reach the extreme values, providing that the variation in temperature is slower than 30°C per minute. These factors show the importance of determining the accurate thermal conditions – both maximum static temperature and cycling parameters – at the solder joint layer.

Variation of the external (outside of the equipment enclosure) ambient temperature is one of the multitude of factors that will determine the actual temperature cycle a specific surface mounted device will see in operation. Very simple equipment, powered continuously at constant power will see the same temperature swings as the external ambient. In some cases, the system designer introduces built-in means of reducing the temperature swing inside the cabinet, such as fans activated when the inlet air temperature exceeds certain limits or inlet air heaters which are activated when inlet air temperature drops below certain limits.

In many applications, the variation of the temperature inside the electronic enclosure is generated by variations of the power dissipated by the electronics itself. Examples of this type of behavior are on/off periods for the system or fluctuations in the power dissipation as in telecommunication equipment due to variations in the number of simultaneous calls passing through the system. Relatively large temperature variations could be generated inside the system between the periods with high traffic, mainly during the working hours, and the periods with low traffic, usually evening or night hours, even though the system is maintained inside an air conditioned room with practically no ambient temperature variations. A device mounted downstream of a high power dissipator sees a temperature variation related to the variation of the temperature of the thermal wake produced by the power dissipator even though the temperature inside the enclosure is maintained constant.

In most applications, the temperature variations at a particular component in a system results from a combination of system-external and system-internal temperature variations combined with power dissipation fluctuations within the component. It follows that different devices inside the same system might be subjected to very different temperature cycles. In order to assess the reliability of the solder joints, the designer must perform a complete thermal analysis at the device level.

D-2.0 THERMAL ANALYSIS AT THE DEVICE LEVEL

The best way of understanding the different factors that impact the device temperature and implicitly the system reliability, is to express the junction temperature on the silicon, T_j, as a summation of temperatures rise at different levels of integration in the system

$$T_j = T_a + \Delta T_{CA} + \Delta T_{BL} + \Delta T_P + \Delta T_{TW}$$

These factors are discussed in D-2.1 through D-2.5 below.

D-2.1 The Ambient Temperature of an Electronic System (T_a) The ambient temperature of an electronic system is defined as the average temperature monitored outside the

system enclosure. It represents the temperature of the ultimate heat sink towards which the entire energy of the system is evacuated, and it represents the lowest temperature of reference. The ambient temperature is different for different types of applications. It can be a near constant as for implanted medical equipment, or it can vary over a wide range of temperatures as for automotive, military or space applications. For any specific case, this temperature is dictated by the application and cannot be modified by design.

D-2.2 The Temperature Rise of the Cooling Agent at the Device Level (T_{CA}) Except for some space applications, the heat dissipated by device is transferred first to a fluid cooling agent which transports the energy outside the system to the ultimate heat sink. For most of the applications the cooling agent is air which comes in direct contact with the device. The mechanism of heat transfer is conjugate convection conduction: part of the heat is transferred direct to the fluid, part is spread first into the solids (board, enclosure) and from there to the fluid. In most cases the temperature of the fluid reaching the device is higher than the ambient temperature (the temperature of the ultimate heat sink) due to the fact that the fluid already absorbed some energy from other devices mounted upstream in the system. The designer has the power to modify this term by modifying the device position in the system or by introducing additional cooling/heating elements in order to moderate dangerous high/low absolute temperature values or strong temperature swings. The temperature rise of the cooling agent is also reduced if the mass (volume) flow of the fluid is increased.

D-2.3 The Temperature Rise Inside the Device Boundary Layer (T_{BL}) The temperature rise inside the device thermal boundary layer is related to the case-to-ambient thermal resistance of the package. A certain gradient of temperature is necessary in order to maintain the heat flow from the package into the fluid acting as a cooling agent. For devices dissipating less than 300 mW, this gradient of temperature (the difference in temperature between the package to the surrounding fluid) is less than 5°C. This is probably the reason that most designers have the tendency of ignoring this term, focusing on the temperature rise of the cooling agent at the device level as the critical factor of ensuring the device functionability and reliability. As the power per device increases, the temperature rise inside the device thermal boundary layer becomes a critical factor. For devices dissipating more than 1 W, this term alone could be higher than 30°C and is certainly one of the dominant terms in predicting the silicon junction temperature.

The designer has the capability of controlling the temperature rise inside the device thermal boundary layer by increasing the local fluid (air) velocity, by using heat spreaders or increasing the substrate thermal conductivity.

D-2.4 The Temperature Rise Inside the Device Package (T_P) Sometimes called junction-to-case temperature rise, this term represents the temperature difference between the silicon chip and the external temperature of the device package. Being related to the thermal conductivity of the materials used for packaging, this term can be controlled by proper selection of materials and use of materials with enhanced thermal properties. For devices dissipating high powers (more than 0.5 W), the resistance of the interfaces between different layers of materials (contact resistances) becomes significant and discontinuities, delaminations and voids could add up to significant thermal resistances.

D-2.5 Thermal Wake (T_{TW}) The thermal wake factor should be considered when devices are mounted close together and their thermal boundary layers intersect with each other. This is particularly important when a sensitive device is mounted downstream from a high power dissipator. Under such conditions the device is engulfed inside the thermal plume of the upstream device. Even though this term is generally low (lower than 5°C) it can produce significant problems if the layout of the board is not carefully controlled.

D-3.0 DETERMINING THE SOLDER JOINTS TEMPERATURE SWINGS

Considering the multitude of factors which determine the device temperature, it can easily be seen that variation of the ambient temperature alone is an indication of the actual temperature variations the solder joint will see in the field conditions. Assuming the temperature of the solder joint is almost identical with the external temperature of the package (case temperature), the temperature cycling is generated by two factors:

a) the variation of the local environmental conditions for the considered device (sometimes called adiabatic temperature or the temperature of the device with power off)

b) the variation of the device power, which in turn produces variations of the temperature rise inside the device thermal boundary layer.

The device adiabatic temperature is the equivalent of the local ambient temperature for a specific device inside the system. It is defined as the temperature that an element achieves when the convective heat from the element to the fluid goes to zero. When conduction and radiation from other elements is negligible, the device adiabatic temperature is the temperature achieved when no power is applied to the device and the rest of the system is activated.

The variation of the device adiabatic temperature is the real temperature cycle that a device operating at a constant power will see inside the system. The temperature cycle could be very different for different devices inside the same system, even though the external ambient is the same.

When variations of dissipated power are involved, the temperature swing related to the power cycling must be added to the variations of the device adiabatic temperature. When the difference in temperature between the device case and the board underneath the device is small (not larger than 5°C), the simple superposition of the two cycles (local environment and power cycling) is quite adequate for estimating the real temperature cycle the solder joint of a specific device will see in different environments and under different operational conditions.

D-4.0 COOLING OF ELECTRONIC EQUIPMENT

D-4.1 Radiation Cooling PWAs by radiation is not practical as a primary heat transfer mechanism because of the large temperature differences required for appreciable heat transfer. In addition, control of heat paths is difficult due to scattering of radiant energy. In fact, radiant heat transfer is potentially objectionable because of the possible heating of near-by temperature sensitive parts by hotter, less sensitive components. The positive effects of radiation from SMT printed boards can usually be neglected.

D-4.2 Free Convection There are some commercial SMT applications which could effectively utilize free convection, although even with free flowing ambient air, the packaging density would need to be decreased, with at least 5 mm, and preferably up to 20 mm spacings between vertically oriented boards, with heat concentrations of no more than 12,000 W/m^3 correspondingly, about 300 W/m^2 of board area dissipation, based on the component side of the board only; for boards with components on both sides, a rough guideline would be 230 W/m^2 per side, maintaining 12,000 W/m^3 maximum.

These numbers for free convection printed board dissipations are relatively insensitive to the variations of printed board size and calculated heat transfer coefficient and hold for an air-to-board ΔT of 40°C. For sufficiently cooler air or hotter board temperatures, greater dissipations can be accommodated. For example, if a 60°C ΔT was acceptable, then 60/40 = 1.5 times as much dissipation could be allowed. A detailed design utilizing conduction spreading of heat within the board should be performed around hot spots in free convection designs to insure maximum junction temperature limits are maintained.

For SMT boards in military applications, free convection is typically a second order effect in removing heat directly from the board. This is especially true when, as would be expected for SMT, that the boards are densely packaged in a structure.

D-4.3 Direct Forced Convection Forced ambient air directly over the board and components, is the most widely utilized commercial method for cooling SMT (and high density) printed boards. Forced conditioned or closed loop air is also common in many military applications. The penalties for this effective cooling mechanism is expenditure of energy, added heat, weight, and volume, taken at the enclosure or system level. The SMT printed board designer will work to the requirements defining air flow rate and temperature over the module, as well as possible variations for altitude, in airborne applications.

Typically, 4 to 8 times as much heat can be removed with forced convection compared to free convection. As a result, heat dissipations in the range of 1500 to 3000 W/m^2 of component side printed board area can be achieved with an average module-to-air ΔT of 40°C.

D-4.4 Conduction Cooling SMT printed boards built with conductive substrates or "cores" such as beryllium oxide, aluminum, or one of several materials designed to match the expansion rate of ceramic components (about 6 ppm/°C), can and should be conductively coupled to the supporting structure by clamping the edges.

The allowable heat densities are significantly greater than those of free convection, and are a strong function of substrate material, thickness, location of heat sensitive parts and conduction paths of these parts to the substrate. The boundary condition may be the temperature of the printed board module substrate edge, or possibly the structural surface to which this edge mates. In the latter case, the printed board designer is dependent on the design of the structure for the interface resistances, a key parameter in the conduction path to the ultimate heat sink. For a 40°C device junction-to-module edge ΔT, dissipations on the order of 250,000 W/m^3, or for a specific module, on the order of 4,500 W/m^2 can be maintained.

D-4.5 Heat Pipes The heat pipe is a thermal conductor of very high conductivity. It is essentially a closed evacuated chamber lined with a capillary structure or wick. Heat is transported by evaporation of a suitable volatile fluid, which is condensed at the cold end and returned by capillary force to the hot end. The vapor passes through the cavity. Heat pipes can be constructed in practically an endless number of configurations, but always consist of three zones or sections, namely: the evaporator, condenser, and the adiabatic section connecting the other two. In some designs, the adiabatic section may be very short.

Thermal resistances of 1°C/kW can be obtained and heat in excess of 50 kilowatts can be transferred. Heat pipes offer important advantages. First, a heat pipe has several thousand times the heat transfer capacity of the best heat conducting materials on a weight and size basis. Second, heat pipes exhibit an essentially uniform temperature at the heat input end. Third, the areas and configurations of contact at each end of a heat pipe are independent and can be designed separately to suit the application.

Fourth, a heat pipe can transfer heat up to several feet with a very small temperature drop. Fifth, a heat pipe can be made entirely of insulating material to provide electrical isolation for high voltage equipment. Sixth, heat pipes require no power for their operation, since capillary pumping is provided by the heat being transferred.

Heat pipes can be designed for operation at any temperature pertinent to cooling electronic equipment. In general, they must be designed specially for each application. One of the major difficulties in heat pipe application is in achieving adequately low thermal resistances at the interfaces at the heat pipe ends. Also, the capillary pumping in a heat pipe is influenced by gravity and external forces. Some heat pipes have exhibited as much as an order of magnitude change in internal thermal resistance due to gravity (i.e., transferring heat downward vs. upward). Further heat pipes exhibit startup difficulties because enough condensate must collect to saturate the wick before pumping can be initiated. If a heat pipe is overloaded, it can rupture.

D-4.6 Direct Liquid Cooling In utilizing direct liquid cooling as an alternative cooling technique, much more is involved than merely replacing the internal air with a liquid coolant. The full effects of the coolant intimate contact-thermal, electrical, chemical, and mechanical must be evaluated, both from a circuit and from a component viewpoint.

The primary effect from a circuit viewpoint is, of course, electrical, and involves the breakdown voltage (dielectric strength) of the coolant in high power applications, and the dielectric constant of the coolant in higher frequency applications. In addition, the fluid selected must not be adversely affected by the electrical fields or voltages normally produced in the equipment.

Components must be carefully screened to insure compatibility with the coolant. The electrical effect on normal air-dielectric components such as trimmer capacitors is obvious. Chemical compatibility with component cases, circuit board material, rosins, and potting compounds, and any other internal module material must be verified. Plastic encased semiconductors are susceptible to leakage in some fluids when the parts are immersed directly in the liquid.

D-4.6.1 Direct Natural Convection Liquid Cooling In direct natural convection liquid cooling systems, it is necessary to expose a maximum of the surface of the heat-producing parts to the coolant and to direct the free convection currents of the fluid around these parts. Thus, in liquids, as in air, parts should be mounted to promote convective cooling. Metallic conduction paths of low thermal resistance from the heat production parts to the surface of the case are not as important in direct liquid-cooled assemblies as in most other types of assembly since adequate cooling is usually obtained by convection. The parts may be supported by solid insulating materials so long as the fluid is permitted to freely circulate around the parts.

Where applicable, the part should be mounted such that the longer part dimension is vertical. The construction of this type of equipment must be given special consideration. With viscous coolants, a slight mechanical advantage is gained by the immersion of the electronic parts in the fluid, since the fluid tends to lend support to parts. Also, it can provide a damping action which assists in resisting vibration and shock, dependent upon the viscosity of the fluid. Generally, the lowest thermal resistances from the parts to the coolant are obtained with direct liquid cooling.

An accurate quantitative analysis of the temperature distribution within a sealed direct liquid cooled system is usually very difficult to obtain, due to the indeterminate overall nature of the circulating convection currents. Nevertheless, at least a qualitative inspection should be made with regard to parts placement. Thus, temperature-sensitive parts should not be placed where they would be in the convection current generated by a high dissipation part. Usually, a temperature gradient will exist in a direct cooled module, with the lowest temperature at the bottom.

Therefore, the more sensitive parts should be placed in the lowermost locations. Holes can be provided in subchassis to direct the flow of the free convection currents around the heat producing parts. The use of direct liquid cooling should not be considered a panacea for thermal problems. The effectiveness of the contained coolant depends primarily on the generation of auto-convection currents. Parts placement should recognize this requirement and not interfere with circulation. Printed wiring boards should be mounted vertically, since a horizontal orientation would restrict the convection currents.

While direct liquid cooling generally allows an increase in parts density in a module because of improved thermal paths, the increase in packaging density is limited by the space requirement for allowing adequate circulating convection currents to develop. Sufficient gaps must be provided between adjacent vertical plates to insure liquid flow, i.e., between a circuit board and a structural wall. Liquids may be as much as 10 times more effective than natural convection in air, allowing up to 3000 W/m^2 board dissipations at a 40°C component to bulk fluid temperature.

D-4.6.2 Direct Forced Liquid Cooling Just as increased cooling effectiveness is obtained with forced air as compared to free or natural air convection, forced circulation of the coolant greatly increases the cooling rate when liquid cooling is used.

In direct forced liquid cooling, part layout and location are most important. The cooled liquid, or that coming from the

heat exchanger, should be directed to cool the temperature-sensitive parts first, and later be directed adjacent to the higher power heat producing parts.

D-5.0 PRODUCT THERMAL DESIGN

The data for thermal resistance of junction-to-air, θ_{ja}, and of junction-to-case, θ_{jc} should be available for all significant power dissipaters.

Time and money can be saved with thermal simulation, analysis and prediction programs on printed board and PWA when those prediction programs are verified by thermal analysis data taken with IR imagers or thermometers.

Thermally sensitive components should be identified. These would include technologies with maximum rated junction temperature $T_j \leq 85°C$, such as high speed CMOS and gallium arsenide (GaAs) with aluminum metallization electromigration limitations or time-dependent-dielectric breakdown mechanisms.

Where there are thermally sensitive components, heat dissipaters should generally be "downstream" in the air flow; under certain conditions of PWA geometry, component orientation and relative component heights, turbulence may result in "recirculation cells" conveying heat "upstream."

Where there are thermally massive heat dissipaters and fans are required to cool the system, the design review should include such items as component T_j "overshoot" on fan turn-off.

Heat dissipaters should generally be "upstream" of tall components to avoid recirculation cells.

Heat dissipater review should include those capacitors with significant ripple current and ripple voltage; the data should include Equivalent Series Resistance (ESR) vs. ripple current, temperature, and frequency.

Where lower T_j is required, should be considered the following avenues particularly applicable to SMT: thermal vias, thermal solder joints, thermally conductive adhesives from component to printed board, and power and ground plans included in the thermal design. In addition, consider the following moves: sensitive components "upstream" of power dissipaters, power dissipaters further apart to reduce power density, power dissipaters closer to cold wall (edge of card if card clamps are used), and power dissipaters "upstream" of tall components.

To allow computation of the reliability of solder attachments (see Appendix A), component lead flexural compliance data should be available for the larger components or for the components with stiffer leads; the critical package dimensions and environmental temperature swings should also be known.

Long, tall components such as connectors are ideally placed parallel to the airflow. Placement of these components perpendicular to the airflow results in the generation of recirculation cells which reduce the heat transfer from heat dissipaters or which increase heat transfer to heat sensitive components.

Software for SM PWA and thermal design exist that allow the designer to perform printed board thermal analysis together with component junction temperature and reliability prediction; some of the programs also address vibration, fatigue, soldering, transmission line/parasitics aspects of printed board design. Other programs perform thermal predictions on printed wiring boards, enclosures, heat sinks, and plates, considering conduction within a printed board, air temperature above components, and full convection and radiation (steady-state and transient). Specialized programs exist for computation of heat sink, heat fin and cold plate performance, under steady state and transient conditions. Powerful computer simulation programs run on engineering computers or PCs for airflow thermal analysis of electronic equipment cabinets or mixed fluid flows.

D-5.1 Component Level Cooling SM components are low profile compared to through hole (TH) components and are therefore more sensitive to the height of surrounding components and their airflow "shadowing" effects. Also, the SM component has no airflow between the bottom of the component and the printed board; the heat transfer in this area is by conduction through the air.

Guidelines on placement of components based on two dimensional airflow simulations and models do not apply to typical SM PWAs. Under natural or low air flow forced convection conditions, heat dissipaters should be "downstream" from thermally sensitive components. Taller passive, temperature-insensitive components should be "downstream" of heat dissipaters, and heat dissipaters should not be in the airflow "shadow" (recirculation region) of taller "upstream" components. Recirculation regions result in a decrease in the heat transfer coefficient of the heat dissipater and an increase in temperature of the other component(s) sharing the heated recirculated airflow.

Under high flow forced convection conditions, recirculation cells can form upstream of a taller, wider component and reduce its heat transfer coefficient or unexpectedly increase the temperature of upstream parts. It helps to turn the long axis of the component parallel to the air flow, to avoid stacking such components end to end perpendicular to the air flow, and to increase the distance to upstream parts. Low frequency oscillations in air flow and subsequent variations in component temperature may result under some circumstances of parts orientation, heat dissipation and air velocity.

D-5.2 Hot Parts (Thermal Considerations) Common methods for controlling thermal rise of our electronic assemblies is forced air, liquid cooling systems or natural

convection. For most products using low power devices, strategic placement of a few ICs and careful venting in a housing or enclosure is adequate. For the products used in a friendly environment, such as the typical air conditioned office, one board assembly will survive indefinitely. But as the complexity and component density increases, creative thermal management techniques must be adopted.

Transferring heat from the component body of ICs and power regulators usually requires some form of physical contact to a mass of material attached to the device. Using hardware or thermally conductive adhesives, as shown in Figure D-1 is a common practice for thermal management. The thermal rise can be distributed to a larger surface area, thereby keeping the component within a recommended operating temperature range. The efficiency of this dissipation and distribution is reliant on the area of the heatsink mass and the loss expected through the interface media. When attachment hardware is used, a thermal compound is applied to prevent air, moisture and contaminants from forming between surfaces. When epoxy attachment is necessary, a thermally conductive material is chosen. The most efficient thermal conductive epoxy usually contains an electrically conductive filler. When maximum insulation is also critical, the heat transfer efficiency from the component to the heatsink will be reduced. Researchers are working on new compounds each year to further improve these thermal transfer characteristics, and heat transfer techniques for through hole devices are as varied as the engineer's imagination.

Care must be taken that the thermal planes do not cause tensile loading of the solder joints.

Typically signal layers on a printed board board are etched in ½ ounce or 1 ounce copper clad dielectric. But 2 and 3 ounce copper is also available for use on power and ground layers. Of course, if the heat transfer is a mechanical attachment to the chassis, the ground plane or planes would provide a thermal conduit to transfer the heat from the component's body into the internal copper layer of this substrate. When specifying the copper thickness on each side of one dielectric layer, the layers and copper thickness should be distributed evenly as the example in Figure D-1. A non-symmetrical lamination may warp excessively during reflow solder process.

The thermal rise expected from the components must be determined, and if this collective temperature rise is beyond the recommended operating temperature limits of the device; a careful evaluation of the component grouping is in order. Distribution of higher power devices on the outer edge of the substrate panels will provide the necessary correction to control and distribute thermal rise away from the components. The more direct the thermal path is away from these components the better; don't locate high power devices in the center of the substrate. Rather, place

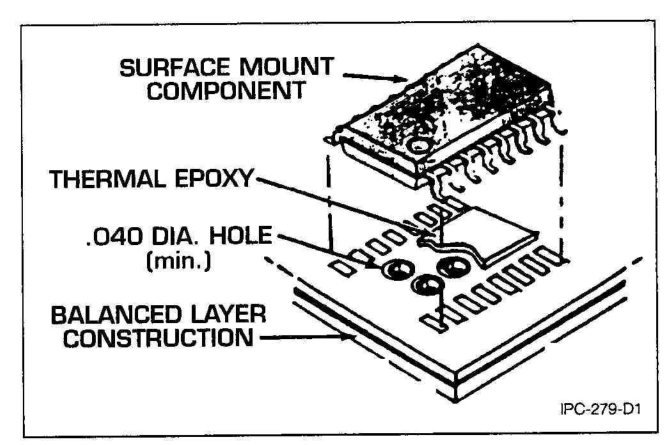


Figure D-1 Thermal Vias and Planes

them closer to the heat transfer edge leaving low power devices in the center area. See figure D-2.

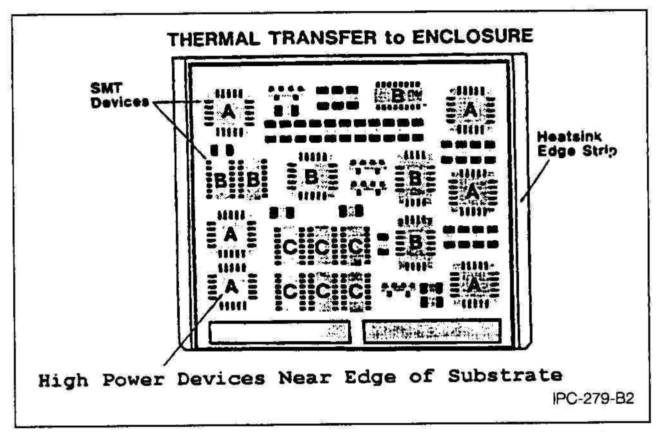


Figure D-2 Other Methods of Conductive Heat Transfer

Figure D-3 describes techniques used to transfer thermal rise of a SMT device through the outer dielectric layer of the printed board to an internal ground plane of metal core. Multilayer printed boards may have power and ground planes internally layered and intermixed with signal layers. This mass of copper planes can be an efficient thermal conductor to transfer heat to the outer edge of the substrate or the chassis.

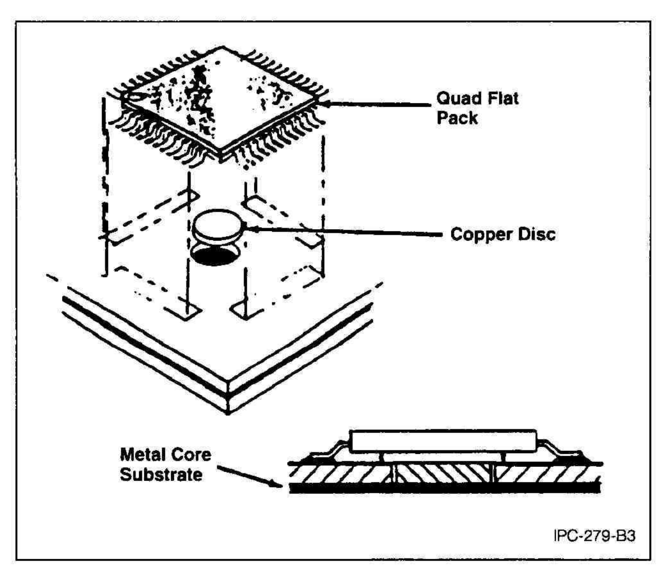


Figure D–3 Use of Heat Slug

Appendix E
Environmental Stresses

The printed board assembly starts its exposure to environmental stresses during bare board fabrication, assembly and repair/ rework before it even enters the service environment. These stresses can be thermal, chemical, mechanical or electrical in nature. It is important to understand the impact of environmental stresses to assure the reliability of the assembly during its service life.

E-1.0 THERMAL

E-1.1 Effects of Rework and Repair "Touch up" is the application of heat and solder to a solder joint which is deemed cosmetically imperfect. Rework is the correction of a defect before the SM PWA leaves the plant. Repair is the correction of a defect found in the field. Information on rework and repair may be found in IPC-R-700. Each correction requires the heating of one or more solder joints above the liquidus temperature of lead-tin eutectic solder (183°C), typically above 210°C, and may involve the removal and replacement of a component. Note that this temperature of 183°C is well above several critical temperatures in a SM PWA.

E-1.2 Glass Transition Temperature for Printed Boards The glass transition temperature (T_g) of most epoxy-glass boards is ~125°C. For multi-functional epoxy glass boards, T_g is ~160°C. T_g is greater for polyimide glass printed boards which have a T_g of 250°C. There are many other printed board materials that fall between these two extremes. Exceeding the T_g of the printed board results in significant expansion of the printed board in the z axis, hence in stresses in the barrels of plated through holes and vias; the result can be intermittent or permanent opens. The intermittent opens can generally be detected during temperature changes of the PWA (see Appendix B).

Printed boards with a lower T_g such as epoxy-glass boards when heated locally, during component removal or component replacement, to temperatures > T_g, will tend to bulge in the heated area. The solder joints of the replacement component will be under tension and may fail when the assembly cools down.

When using hot gas or IR systems to remove or replace components, minimize printed board time at temperature.

During component removal, there should be no component lifting or twisting during removal until solder is liquid on all lands. This minimizes stress on the leads where they enter the component package (with the result of cracked plastic package body, damaged glass to metal seals), as well as stress on the lands and their adhesive bond to the printed board (with the result of lifted lands).

E-1.3 Intermetallic Compound Growth The copper in the printed board conductors and component leads reacts more rapidly with the tin in the solder to form a brittle intermetallic compound (IMC) such as Cu_3Sn and Cu_6Sn_5 at higher temperatures. The original eutectic solder will be transformed into a lead-rich layer. In the worst case, the surface is exposed and oxidized; this lead oxide rendering that surface unsolderable.

A solder joint kept at temperatures exceeding 150°C will result in a lead-rich joint which is less ductile than one with eutectic solder and the fatigue life of the joint will be degraded. The IMC layer will tend to act as a shear plane under overload conditions. These comments apply to neighboring joints during component removal or replacement and to "touch up" of a joint; some data indicate that solder joints which undergo a "touch up" are less reliable.

If the molten lead is removed from the land by wiping, the exposed IMC layers can rapidly oxidize and become unsolderable.

If the heat source is solder (wave or fountain), the intermetallics will be carried away and in the extreme, the copper land will be dissolved.

When using hot gas or IR systems to remove or replace components, keep the heat away from neighboring components and joints. Hot air deflectors and IR shielding panels may be required for component protection.

E-1.4 Glass Transition Temperature for Plastic Encapsulating The T_g range of most molding compounds used in the plastic encapsulation of semiconductors and passive networks is in the range of ~150°C to 180°C.

Exceeding the T_g of the moulding compound of the components during component removal results in internal stresses to the metallization and passivation of the silicon chip. This damage can hinder failure analysis of the removed component and can also be suffered by a neighboring component. Disruption of the metallization can result in opens and dysfunction of the chip. Damage to the passivation can result in long term corrosion of and opens in the metal. Exceeding the T_g can also cause delamination of the molding compound from the surface of the silicon chip or the surfaces of the leadframe; condensed moisture can pool in the delaminated sites and lead to dendrites and corrosion. Where the delamination coincides with bonding pads and wire bonds, bond shear can occur.

When using hot gas or IR systems to remove or replace components, if subsequent failure analysis is to be performed on the removed component, dry the component

prior to removal. Keep the heat away from neighboring components and joints with hot air deflectors and IR shielding panels.

E-1.5 Water Vapor Pressure Effects on Plastic Encapsulated Components Condensed water vapor at the interfaces within a plastic encapsulated surface mount component (PSMC) rapidly turns into steam and can cause delamination between the moulding compound and various elements such as the leadframe, the bonding fingers, or the chip/die surface. This phenomenon normally occurs at ~220°C. In extremely susceptible components, the threshold temperature is expected to be lower than 220°C. In the worst case the delamination of the molding compound can progress to a continuous crack between the die and the exterior surface of the package, permitting materials such as flux and cleaning solvents to enter the package.

These materials, in the presence of water, corrode the metallization of the die; in the additional presence of DC bias, dendrites can form between conductors. Even when there are no external cracks, ionizable substances can be extracted from the moulding compound or from the surface of the chip (such as from phosphorous doped oxide); these materials, together with condensed water are trapped in the delaminated regions and, over time, result in corrosion and dendrites (see Appendix C).

When using hot gas or IR systems to remove or replace components, particularly if subsequent failure analysis is to be performed on the removed component, dry the component prior to removal. Hot air deflectors and IR shielding keep the heat away from the neighboring components and joints. Where hot gas or IR has been used to remove a component and the body temperature has exceeded ~260°C for 10 seconds, the re-use of that component is not advised, particularly if the component is susceptible to plastic package cracking and has not been dried out prior to removal. Characterize replacement parts for plastic package cracking susceptibility by the procedures in IPC-SM-786 or IPC-TM-650, method 2.6.20.

E-1.6 Water Vapor Pressure Effects on Printed Boards The glass-epoxy or glass-polymer interface can separate or delaminate, resulting in "measling" when heated above ~260°C for extended periods. This phenomena occurs at the 260°C temperature for glass epoxy boards and lower temperature in glass polyimide boards that have been exposed to moist environments. Conductive anodic filaments (CAF) can form low or high resistance conductive paths between the barrels of the PTVs (vias) or PTHs (plated-through-holes) where the measling has occurred. Most glass-polymer printed board materials should have been evaluated at 260°C for measling during the "solder float test." Increased susceptibility to measling or delamination is noted when the polymer has a significant moisture content; polyimide or polyimide based substrates should be dried prior to high temperature exposure.

When using hot gas, IR, or manual iron systems to remove or replace components, oven dry the substrate at 125°C for 24 hours prior to high temperature exposure and minimize printed board time at temperature. Use thermometry to measure and control the temperature of the substrate and the component during removal and replacement; gas stream temperatures > 350°C have been noted in systems setup for rapid component removal.

E-1.7 Solder Melt Temperature Effects At the temperatures required to melt solder, the adhesive binding the copper conductor to the printed board weakens. Aggressive use of a soldering iron to move or remove solder or to move a component lead by lifting, prodding or twisting before the solder is completely melted can result in the bending, tearing or complete failure of both external and internal lands or conductors; conductor repair is then necessary. The same land or conductor damage follows premature lifting or twisting of a component prior to complete solder melting.

During component removal and rework/replacement, such as on connectors and PGAs with fountain solder, minimize the exposure of the printed board to the molten solder. Alternatives are to employ thicker copper plating or nickel barrier plating to minimize the effects of copper dissolution, particularly on the PTH or PTV knees.

E-1.8 Temperature Excursion (T) and Temperature Rate of Change (T/t) If molten solder contacts the termination of a multilayer ceramic capacitor (MLCC), multilayer ceramic inductor, or multilayer ceramic filter network, during "touch up", rework or repair, and results in a thermal transient exceeding 4°C/second, a crack may result. The crack occurs in the ceramic body under the termination, hidden from visual inspection but capable of being a site for dendriting under conditions of moisture and bias. Most MLCC suppliers recommend a $\Delta T < 100°C$. Some soldering irons, set at 425°C, with sufficient thermal mass in the tip, and with a tip wet with solder will transfer heat so rapidly that the ceramic under the termination will crack. Preheating of the component above 150°C may be required to avoid this kind of cracking but may result in damage to other components or the printed board. The issue of thermal shock cracking for MLCCs is worse for capacitors with high values and high thickness; other parameters which correspond to thermal shock susceptibility are high layer count, high dielectric constant or low working voltage rating. Require your component supplier to provide data regarding the ΔT and $\Delta T/\Delta t$ to which the particular capacitor (dielectric type, value, working voltage case style, temperature coefficient of capacitance) is robust; this data may restrict your choice of component values (parameters) or suppliers.

E-2.0 CHEMICAL

E-2.1 PWA Cleanliness Where water soluble or other fluxes are used, assure that the PWA is cleaned at least to the ionic contamination levels expected of a first-pass board. Otherwise, long term failure mechanisms may result. Corrosion stress cracking of the solder joints may occur, together with dendrites on the surface of the printed board and loss of Surface Insulation Resistance performance (particularly important in high impedance linear applications). See also the comments on cleaning under "Conformal Coating".

E-3.0 MECHANICAL

E-3.1 PWA Flexure Excessive flexure of the PWA due to shock, vibration or handling during rework or repair can result in a cracked component body, a detached termination, or an overloaded and failed solder joint.

E-3.2 Tooling Impact Impact of a hard tool on a ceramic component body or termination can result in a cracked or fractured component body.

During component removal, there should be no mechanical stress on neighboring components. Some removal techniques and tools have been observed to use a neighboring component as a pivot or fulcrum.

E-4.0 ELECTRICAL

E-4.1 Electrostatic Discharge (ESD) Observe ESD precautions while handling, testing, and transporting the PWA to avoid the introduction of infant and latent defects.

E-5.0 SMT FAILURES/STRESS CONDITIONS

E-5.1 Component Derating Reference Conditions Component derating is commonly referenced to the absolute maximum ratings defined by the manufacturer's specification or data sheet. Each of the several maximum ratings (e.g. power, voltage, current, temperature) must be applied individually and not in combination with any other absolute maximum rating. Where experience dictates, more conservative references may be used.

E-5.2 The Most Important Stress and Some Precautions The most universal stress is temperature. The critical point at which to evaluate temperature is the active site or junction or film, not the ambient temperature; this definition of the critical temperature takes into account the temperature rise in the component due to heat generated within the component. Many of the common failure mechanisms in electronic components double their failure rate contribution with an increase of only 10°C.

Caution The absolute maximum ratings or the temperature/thermal derating of components usually state or imply a maximum operating and/or storage temperature (whether junction or hot-spot) and various electrical values based upon DC power conditions measured in a still ambient at 25°C. However, to determine whether this assumption is true for specific components, you may have to question the manufacturers' engineering staffs.

The physical configuration of the test environment is often not specified; this failing most affects low, short-leaded components such as those in SMT because of unstated significant factors such as the orientation of the component, the printed board conductor configuration, the use (or non-use) of sockets and the velocity of the airstream immediately adjacent to the component under test.

E-5.3 Failure Modes/Failure Mechanisms A failure mode is the failure of a component to perform its electronic or mechanical function. An electronic component fails due to the underlying chemical, physical or mechanical mechanisms.

For instance, an integrated circuit (IC) can fail due to an open failure mode on a given pin or lead.

The responsible failure mechanisms can include: external lead contamination leading to an open solder joint; lifted bond wire at the internal package lead; corroded wire in the package; resistive and brittle intermetallic compound (IMC) growth at the wire/package interface; broken bond wire (due to cyclic fatigue from external temperature cycling, cyclic fatigue from internal power cycling, tensile overload, material coefficient of thermal expansion incompatibles), melted bond wire (due to high currents); lifted bond wire at the integrated circuit die (due to a poorly executed bond, corroded bond pat metallization, contamination on bond pad metallization, excessive IMC development); open IC die metallization (due to poor oxide step coverage, electrical overstress, electromigration, corrosion, stress from dielectric layers, or stress from molding compound movement). Note that these mechanisms can be the result of simultaneous or sequential exposure of the component to the physical/mechanical, chemical or electrical stresses.

E-6.0 OVERVIEW OF STRESSES

E-6.1 Common Stresses and Component Response to Stress Thermal stresses include static high and low ambient temperature and cyclic ambient temperature; power cycling results in cyclic internal temperatures. Cyclic temperatures result in thermo-mechanical stresses. Electrical stresses include static and cyclic power; static, cyclic and transient voltage; current and current density; electrostatic discharge (ESD) and electro-magnetic interference (EMI). Chemical stresses include moisture or humidity, corrosive

gas ambient, hydrolyzable dust and sand, solvents and residual hydrolyzable contaminants from the fabrication and assembly processes and handling. Mechanical stresses include sand and dust, mechanical shock, vibration, connection/removal of connectors, and unrelieved strain due to warped printed circuit boards. Other stresses include low atmospheric pressure/high altitude/vacuum, electromagnetic radiation, ionizing radiation such as X-rays and alpha particles. A special but not uncommon case of a combined stress is that of temperature- humidity- bias.

E-7.0 IMPORTANCE OF TEMPERATURE AS A COMPONENT STRESS FACTOR

Temperature is the greatest single contributing stress to component failure.

E-7.1 Temperature-Related Reversible/Temporary Changes in Component Parameters Examples of reversible changes include:

- increased resistance in metallic resistors
- changes in capacitance, dielectric constant, power factor, and equivalent series resistance (ESR) of capacitors
- decreased inductance of inductors and filters, particularly near Tc (Curie temperature)
- increased gain of bipolar transistors
- decreased breakdown voltage and increased saturation (leakage) current of P-N junctions
- increased output resistance of bipolar and field effect transistors
- decreased viscosity and load carrying ability of lubricants.

High temperature exposure during SM assembly processing (particularly solder reflow) or service also results in reversible

- expansion of materials (particularly of polymers above T_g) with the possibility of the jamming of moving parts and the "bi-metallic" bowing of materials
- loss of control and a long recovery period in temperature stabilized components such as crystal oscillators.

E-7.2 Temperature-Related Irreversible/Permanent Changes in Component Parameters Examples of irreversible effects of exposure to high temperatures include the following:

- oxidation (particularly of lubricants and contacts)
- corrosion (particularly in the presence of moisture and hydrolyzable contaminants)
- Intermetallic compound (IMC) formation particularly in the case of SMT and Tape Automated Bonded solder joints and other bi-metallic joints.
- grain growth in multiphase alloys such as eutectic lead-tin solder
- diffusion of alkali metals in semiconductor devices resulting in device instability
- diffusion of halogenated solvents through rubber seals of non-solid electrolytic capacitors resulting in internal corrosion and subsequent component failure
- evaporation and subsequent loss of high vapor pressure fractions of silicone compounds, greases and fluids
- evaporation and subsequent loss of plasticizers in plastics
- evaporation and transportation of silicone and plasticizer compounds to the mating surfaces of separable contacts such as those in relays and connectors and cold flow of materials such as polytetrafluoroethylene (PTFE).
- evaporation and subsequent loss of fluid in non-solid electrolytic capacitors has caused losses on components and instruments which have been in storage at room temperatures. Evaporation is accelerated at higher temperatures and higher altitudes. Some aluminum electrolytic capacitors rated for operation from –55°C to +85°C or +105°C contain fluids such as dimethyl formamide (DMF) which has a boiling point of 67°C. Replacement of the DMF with dimethyl acetamide (BP = 74°C) or gamma butyrolactone (GBL) (BP = 97°C) reduces the susceptibility of the component to high temperatures. Because these solvents have flashpoints very close to their boiling point, the solvent change also reduces the fire hazard. Changing from DMF to dimethyl acetamide or GBL also reduces the toxicity of any leaking electrolyte.

High temperature exposure during SM assembly processing (particularly solder reflow) also results in irreversible

- internal and external SM integrated circuit package delamination and cracking, mechanical damage to the surface of the die and its microinterconnections as well as and potential failure due to corrosion of the die metallization. Passive component networks are also susceptible to this delamination, cracking, and corrosion. See appendix D for a summary and IPC-SM-786 for details.
- temporary softening and a degradation in resistance to cut-through of insulating polymers (such as those in capacitors) with a permanent loss of dielectric withstand strength and mechanical strength and a long period to recover some of the lost properties.
- stress cracking of susceptible polymers, such as transparent nylon optical components under internal

(molded-in) or external mechanical stress and particularly in the presence of some solvents (such as condensing alcohol vapor)

- mechanical stressing of components containing materials with mismatched coefficients of thermal expansion (CTE) such as joint stress between a polymer-glass based SM substrate and rigid ceramic components such as large multilayer capacitors, power resistors, ceramic based hybrids, and inductors
- melting and opening of soldered connections internal to capacitors, inductors, crystals, and resistor/capacitor networks
- melting or softening of the polymeric capacitor dielectrics such as polystyrene, polycarbonate (PC), polypropylene, polyethylene terepthalate (PET) with dielectric thinning as a result of the relaxation of winding stresses at high temperature. The thinned dielectric results in uncontrolled increase in capacitance and decrease in dielectric breakdown voltage and a long period to recover some of the lost properties
- expansion of elastomeric materials such as silicone or RTV used for "potting" components (such as optocouplers, pulse transformers, inductors, and delay lines) with subsequent breaking of components, wires and joints
- softening and relaxation of elastomeric materials such as O-rings in variable resistors, with subsequent loss of seal and initiation of corrosion
- softening and cracking of the low T_g conformal coatings of axial and radial capacitors, with subsequent corrosion
- softening and weakening of internal epoxy connections in assemblies such as crystals and hybrid oscillators
- softening, distortion, or deformation of plastic components (such as surface mount connectors and light emitting diode [LED] display scramblers) with loss of dimensional accuracy
- overcuring of polymers used for insulation with a decrease in insulation resistance (IR)
- boiling and evaporation of the fluids in non-solid electrolytic (such as aluminum and wet slug tantalum) capacitors with subsequent loss of capacitance and increased Equivalent Series Resistance.

Identify the maximum allowable internal body temperature (defined by the boiling point of the electrolyte, the softening point of the plastic dielectric), or the softening range of the internal solder joints and match that temperature constraint with the solder reflow profile to prevent component degradation.

See also the comments in this design guide, Appendix A, on the effects of temperature and temperature cycling on solder joint reliability and solder joint fatigue and methods of computing the reliability impact. See also the comments on process and rework temperatures in this design guide, particularly the effects on plastic surface mount components in Appendix F.

E-7.3 Effects of Low Temperature Low temperatures result in:

- loss of flexibility and decreased impact resistance in polymers
- liquid water film formation below dewpoint with subsequent opportunity to induce corrosion
- ice formation with subsequent delamination or melting of the ice
- viscosity increase particularly in lubricants and liquid electrolytes
- contraction of materials with subsequent jamming of moving parts or bi-metallic bowing of materials
- thermomechanical stress of components containing materials with mismatched coefficient of thermal expansion (Δ) joined by SM reflow
- decreased bipolar transistor gain and increase FET transconductance
- stress and rupture of some SM solder masks and other coatings
- loss of control in temperature stabilized components such as crystal oscillators
- increased dissipation factor in "hi-k" ceramic capacitors
- increased stress in encapsulants and molding compounds with subsequent damaged IC passivation, damaged IC metallization, cracked silicon, or induced dark line defects and loss of light output in LEDs.

E-7.4 Effects of Temperature Changes Temperature or thermal cycling can result in:

- repeated stressing of structures and material systems with mismatched thermal expansions resulting in repeated "bi-metallic" bowing and possible fatigue. Particularly susceptible are systems of ceramic and organic components affixed to organic and ceramic substrates, respectively (for instance, where ceramic LCC are affixed to organic FR-4 boards or plastic encapsulated components are affixed to ceramic substrates). The most severe cases can result in component cracking or solder joint failure due to overload. Thermo-mechanical fatigue effects are worse with lower cycling frequencies due to relaxation effects.
- jamming of moving parts
- repeated condensation of moisture
- repeated evaporation of moisture

With significant power dissipation in the component, the effects of the cycling of power dissipation within the component (power cycle) may be more influential than the cycling of ambient temperature, even when the CTE of the component and substrate are matched.

See also the comments in this design guide in Appendix A on the effects of temperature and temperature cycling on solder joint reliability and solder joint fatigue and methods of computing the reliability impact.

E-7.5 Thermal Shock Thermal shock is defined by a rapid temperature change.

Thermal shock can occur during SM solder reflow, wave solder or hand solder. Without adequate preheat, the result is cracked laminated or multilayer ceramic and ferrite components such as Multilayer Ceramic Capacitors (MLCC), inductor and filter networks. Recommended process parameters to avoid thermal shock:

- a $\Delta T/\Delta t < 4°C$/second
- a ΔT of < 100°C from preheat to peak process temperature; noted by most manufacturers for most of their products.

The literature reports variations from supplier to supplier and within a supplier on these "rules."

E-8.0 POWER

The primary consideration of power is the resulting temperature. Roughly

$$(P \times \theta_{ja}) + T_a \gg T_j$$

Where P is the power dissipation, θ_{ja} the thermal resistance from junction to ambient, T_a the ambient temperature and T_j the junction or active film temperature of the component.

θ_{ja} is a parameter value generally averaged over the component package.

Hotspots can occur in semiconductors as a result of delamination or large voids due to poor die attach material or poor die attach process. Hotspots can also occur in semiconductors due to avalanche voltage breakdown and during second breakdown. $\theta_{ja} = \theta_{jc} + \theta_{ca}$, the thermal resistance from junction to case added to the thermal resistance from case to ambient. θ_{jc} is a component package parameter value strongly dependent upon the conditions under which it is evaluated (air flow speed and orientation, resulting laminar or turbulent air flow, etc.).

Cyclic power dissipation conditions result in cyclic temperature fluctuations. Power devices with solder die attach can suffer fatigue of the solder after power cycling, with resulting cracks and delamination of the solder and subsequent increase in thermal resistance and progressive failure.

Excessive ripple voltage or current in non-solid electrolytic capacitors, in conjunction with the equivalent series resistance (ESR), results in internal heating or unexpected power dissipation; this increase in internal temperature increases the evaporation of the electrolytic fluid, increases ESR and results in subsequent failure.

High frequency currents in ferrite inductors also results in internal heating; this effect is exacerbated by high levels of DC current.

See also the comments in this design guide (Appendix B) on surface mount thermal design.

E-9.0 VOLTAGE

Solid dielectric breakdown, a bulk effect, affects the oxides used in integrated circuit dielectrics, MOS device gates, and other junction bipolar passivation; also affected are the polymers used in capacitor, inductor and optocoupler insulation systems. Solid dielectric breakdown also occurs at bipolar junctions such as the collector-base of transistors. The derated breakdown voltage should not be exceeded. Worst case power transient conditions and other such "low probability" occurrences must be considered.

Gas dielectric breakdown occurs between closely spaced unpassivated or uncoated conductors and can result in melting and fusing of conductor materials; the accompanying arcing can also degrade, melt or burn adjacent insulating materials and spray molten materials on those insulating materials. Conduction through a gas may be initiated in such different forms as corona, glow discharge, spark and arc.

Surface breakdown occurs between conductors or between conductors and generally underlying semiconductor and "around" interposed insulating materials; surface breakdown can result in melting and fusing of conductor and semiconductor. In addition to the breakdown mechanisms, voltage bias can result in metal ion migration in dielectrics, with subsequent instabilities in semiconductors (where light alkali metals and ions are particularly notorious) and voiding/shorting in thick film components and assemblies (where silver and palladium shorts have been noted). When the energy release during the surface breakdown event is high enough, the surface may be degraded and the residues may be electrically conductive. Where the surface is the printed board, a parameter such as comparative tracking index (CTI) may be required by regulations.

Cyclic voltage stresses introduce the effects of "equivalent series resistance" (ESR) in dielectric systems; some fraction of the energy delivered to the capacitor expresses itself as heat (Joule heating + dielectric loss) and must be considered in the thermal derating of the component. ESR effects are a function of the peak to peak value of the applied voltage and the frequency of the applied voltage.

In ceramic dielectric capacitors (MLCC) such as those used

in SM, dielectric loss and dielectric constant increases with increased applied cyclic voltage; this effect is more severe with "hi-k" dielectrics.

The acceleration factor (voltage exponent) for capacitor failure rate vs. voltage varies from -3 to -5. That is, time to failure is generally proportional to V^{-3} to V^{-5}; mica capacitors have a voltage exponent of 8. AC voltage stress effects may not be extrapolated from DC or lower voltage test values. Transient effects of voltage surges may not be extrapolated from DC or lower test voltage values.

Ceramic dielectric capacitors, particularly "hi-k" types demonstrate a decrease in dielectric constant and dissipation factor with increasing DC bias voltage; this effect is more severe with thinner dielectric layers.

E-10.0 CURRENT AND CURRENT DENSITY

Conductors have finite resistance and develop Joule or resistive heating at high currents. Where the current density is high and the ability of the conductor to dissipate heat to its surroundings is low, self heating effects may affect the life characteristics of the conductor. Joule heating and ambient temperature effects are the underlying concerns of the current density graphs in IPC drawing IPC I-00005. Note that the graph is indeterminate in range of the 0.1-0.5 mm conductor widths of concern in SM designs. The cross section is quantified in a "square mils" (0.001 inch by 0.001 inch) and a conductor 0.005 inch wide by 0.0005 inch thick is 2.5 "square mils." Conductors covered by solder mask or conformal coating are considered "internal" conductors since the heat dissipation capability is impaired by the overlying electrical and thermal insulation.

Electromigration, normally a long term effect in integrated circuits and semiconductors, occurs when at current densities on the order of the critical current density at the temperature of interest, the metal atoms of the conductor move with the electron wind, forming hillocks/whiskers and leaving voids/cracks. A critical current density at normal temperatures for thin-film aluminum used on ICs is $\sim 10^5$ A/cm^2. The hillocks/whiskers can penetrate dielectrics and cause shorts. The voids/cracks result in opens. See also the notes of the Joint Electron Devices Engineering Council Committee 14.2 on electromigration in silicon semiconductor ICs. At very much higher current densities, the conductor can melt, resulting in an open; where an underlying dielectric also melts, a short can develop between the conductor and a conductive substrate.

The electromigration robustness of thin layers of large-grained copper such as that on printed boards appears to be much better than that of the thin-film aluminum on ICs. Do not use the internal ground connections in IC packages as part of the ground distribution system on the printed board.

E-11.0 ESD/EOS (Electrostatic Discharge/Electrical Overstress)

The result of ESD exposure may be patent (immediately detected) but there is evidence of latent damage where the component is "wounded" with later failure. See also the extensive literature on EOS/ESD in silicon and other components fabricated with thin oxides, thin-metal films and shallow junctions. Data from the tables of ESD susceptibility are in the appendix of this design guide.

ESD melts, modifies or destroys thin oxide layers (such as those used to passivate resistive films and in ICs for passivation or dielectric purposes in ICs), thin-metal layers (such as those found in ICs, thin-film resistors and Surface Acoustic Wave Resonators), thin dielectric layers (such as those used in multilayer ceramic capacitors, shallow semiconductor junctions (such as those in high frequency ICs and discrete devices), and thin polymeric layers (such as those used in plastic film capacitors). The literature reports ESD failures on I/O ICs as well as on ICs connected to those I/O components; the connection of charged cables to instruments is suspected of introducing ESD and EOS associated with complementary metal oxide semiconductor (CMOS) latchup. Longer data lines and faster I/O ICs probably exacerbate these failure modes. Also contributing to sad experiences with latchup are application specific ICs (ASICs) and custom- or semi-custom ICs fabricated with new layout libraries or new processes which have not been thoroughly characterized for ESD and latchup.

The high peak temperatures attained during ESD exposure result in melting or structural changes (e.g. grain size) of the metal or metal/glass films (due to melting or annealing), changing of the value of the resistor and, in addition, degrading of the noise figure (NF) and temperature coefficient of resistance (TCR) of the resistor. Thin-film resistors, more so than thick film resistors, are dependent on grain size and structure for their value and NF performance. Devices of small geometry (due to low thermal dissipation capacity) are susceptible. Thick-resistive films have demonstrated susceptibility to fields of 2 kV/mm. Bulk resistors appear immune to ESD.

ESD also results in melted semiconductor materials, particularly P-N junctions, with subsequent degradation or loss of function. Particularly susceptible are high frequency devices with junctions which are very small, very thin and demonstrate low breakdown voltages.

ESD may be treated as a special case of voltage overstress; the potential may be greater than 10 kV and the duration may be less than 1 msecond; if the source is a human body, the source capacitance may be ~150 pF and the source impedance may be ~1kΩ. Charged cables possess capacitances of 100- 1000's of pF and may be charged to voltages of 100-1000's of Volts; in this energy regime, the damage may appear as EOS of interface ICs.

ESD events can also initiate "CMOS Latchup" with subsequent electrical overstress and no evidence of ESD susceptibiilty. ESD events can induce transient currents into neighboring circuits, causing circuit upset. Characterization of the level of susceptibility of the component to ESD and latchup and the design of circuitry designed to shunt ESD energies away from susceptible components is recommended. Obtain characterization data on ESD susceptibility of thin film resistive components from the supplier; avoid inadvertent damage to sensitive components.

Gross EOS is the cause of many resistor failures due to the failure of some other circuit or due to a surge from an external energy source. To reduce the failure rate of the fielded product due to EOS of resistors as well as other components:

1. Reduce the magnitude of overstress below the catastrophic failure level by modifying associated circuits if possible; voltage regulators with crowbar capability or fold-over regulation may be one method.
2. Reduce the magnitude of consequent overstress below the catastrophic failure level by incorporating circuit elements such as current-limiters, voltage-limiters, positive temperature coefficient resistors or thermal cutouts.
3. Use resistors with higher wattage ratings; better still, use combinations of series or parallel resistors to spread the heat load over the printed board (lower the power density).
4. Use resistors of more rugged materials (metal oxide) in those situations where the resistor is intended to take overstress without damage.
5. Use a part with an overstress failure mode of increased resistance (or open) such as carbon composition, and NOT one which tends to decrease in resistance, such as metal film or carbon film.

Power transistors can suffer from second breakdown (SB) current, a possibly destructive condition which occurs when a hot spot is created within the chip due to high power density in a small volume. This I_{SB} current is a function of the collector voltage and is the value of current at which SB occurs.

E-12.0 MOISTURE AND HUMIDITY

Adsorption of water on surface of insulators with dissolution of hydrolyzable contaminants results in the subsequent loss of Surface Insulation Resistance (SIR), particularly on porous surfaces such as uncoated printed boards. Absorption of water in bulk of insulators with dissolution of hydrolyzable contaminants results in the subsequent loss of bulk moisture insulation resistance (MIR) particularly in printed boards, dielectric film capacitors and plastic encapsulated electronic components such as integrated circuits, networks, and hybrids. Molded or conformally coated packages can absorb water and flux contaminants in soldering and cleaning processes if the package is improperly sealed particularly at the junction of the termination and the coating; to avoid these consequences, use components which are able to pass stringent moisture resistance tests under conditions such as biased 85C/85% RH or biased Highly Accelerated Stress Testing (HAST), after thermal preconditioning simulating the soldering or reflow environment. Absorption of water in the bulk of the insulating film of capacitors results in increased dissipation factor. In presence of water, the oxidation rate of oxidants such as SO_4 and O_2 is increased. In presence of water, the corrosion rate and metal migration growth rate effects of halides such as chloride and fluoride are greatly increased. Absorption of water by specific plastic and gasket materials (up to 1% water by weight) results in swelling; cyclic changes in humidity can result in "creeping" of the plastic or gasket material. Very low levels of relative humidity (RH) allow ESD voltages to build up. In the presence of water and nutrient materials, fungus growth is increased and corrosive organic acids are released. Chemisorption of water into polymers such as molding compounds results in a lower Tg and increased total thermal expansion.

In the presence of water and electrolyte, galvanic corrosion of metallic films and finishes is enhanced. See Appendix L for a tabular listing of compatible finishes. Identify and avoid exposed galvanic couples such as terminations of copper - nickel - gold which are sheared after plating; in addition, exposed base metals on the edges of contacts can lead to tarnish creep, the extension of corrosion products of copper over the gold. Susceptible components include ceramic packages; brazed and plated terminations may have brazed joints of metals constituting galvanic couples, exposed plated interfaces, and have been or need to be trimmed and/or formed after plating. Identify mechanical stress levels in metals (particularly formed terminations) which might contribute to stress corrosion or plating discontinuities; alternatively, form metals in the annealed state and then postplate.

E-13.0 CORROSIVE GAS AMBIENT

The result of corrosive gas ambient is material loss due to corrosion of the metallic conductors, continuity loss due to build up of non-conductive corrosion residues (particularly between contacts) and loss of insulation resistance or shorts due to build up of conductive corrosion residues. See also temperature, humidity section above and temperature/humidity/bias section below.

Salt atmosphere (or spray) and corrosive gas atmosphere are both excellent source of hydrolyzable, conductive contamination + water + oxygen. Salt atmosphere/spray stress is encountered in naval electronics and required in military systems but is not commonly encountered in commercial

situations; the stress normally results in detection of plating porosity, but is also known to result in loss of hermeticity in sealed packages as well as loss of legibility of component marking. The pH at which this test is conducted is significant to the test results.

E-14.0 TEMPERATURE/HUMIDITY/BIAS

The combination of the stresses, temperature, humidity, and electrical bias, in the presence of conductive contamination, particularly halides, results in electrochemical corrosion and metal migration. Metallic dendrites of the common electronic metals (silver, copper, tin, lead, gold) have been found on assemblies during high temperature/high humidity testing; these dendrites occur on the surface of the printed board. Dendrites are found within the bulk of the printed board where voids allowed entrapment of conductive solutions and within delaminated areas of ICs where flux residues were found. Under this combination of stresses and where the bulk of the encapsulating material is the source of the contamination, ICs are found to demonstrate a time to failure described by

$$t_f = (RH)^n \exp\left(\frac{E_a}{kT}\right)$$

where RH is the relative humidity (%), E_a is the activation energy (eV) in the range of (0.77 to 0.81 eV) and n is in the range of -2.5 to -3.0. The RH range around 100% is anomalous. See Appendix C .

Dendrite growth of silver, copper, lead or tin also occurs outside and inside plastic encapsulated integrated circuits and networks. Molding voids; internal and external package cracks at the bonding fingers; manufacturing process damage at trim and form (possible when the component supplier process quality is inadequate); as well as delamination during solder reflow create an ideal physical/electrochemical environment for dendritic growth.

E-15.0 SAND AND DUST

The results of exposure to sand - dust can include increased friction between mating surfaces in disk and tape drives; increased abrasion of mating plated surfaces- where the plated surfaces form an electrical contact, contact failure may be intermittent or complete; contaminated, abrasive lubricants (Desert Storm demonstrated many ineffective air and oil filtering systems); clogged metering orifices of air dashpots; and clogged air filters with reduced cooling efficiency.

Dusts with even slightly conductive constituents can reduce insulation resistance and contribute hydrolyzable contaminants with subsequent effects noted under the moisture/ humidity section above. Highly conductive dusts have been wiped up from the tops of dust hoods in "clean" factories.

E-16.0 MECHANICAL SHOCK

Mechanical shock may excite resonances in systems and printed circuit assemblies. During surface mount technology assembly, mechanical shock can be introduced by pick and place machine collets; broken multilayer capacitors and broken solder joints have resulted. During through-hole (TH) assembly, mechanical shock may be introduced by the TH insertion machine or by the lead trimming process. High energy processes such as depanelizing (routing) have resulted in displaced and broken wirebonds in integrated circuits built with an open cavity around the bonding wires. Peak stresses may overload or plastically deform structures which may then fail by cracking, moving or changing shape. Jamming or impairment of mechanical functions may occur. Momentary disruption of electromechanical functions may occur on disk drive arms, tape drive heads, and relays; momentary opens may occur in switches, connectors, and between components and their associated sockets. Transportation is a source of mechanical shock in service. Inappropriate use of elastomers intended to isolate product from external sources of mechanical energy may result in surprising damage from energy stored in the elastomer.

E-17.0 MECHANICAL VIBRATION

Cyclic peak stress and fatigue lead to loss of strength or material failure such as cracking, brinelling, spalling, or displacement. Mechanical modulation of contacts (sockets, relays, connectors, insulation displacement connection cables...) results in momentary opens and intermittent failures such as no trouble found (NTF). Repeated flexing of materials (cables, joints, 1 piece hinges...) results in work hardening, fatiguing and cracking. Fretting, which is mechanical wear in localized areas due to micromotion, results in continued generation of intermetallic compounds in contact systems where gold plating opposes tin plating, thinned or ruptured plating where a soft metal opposes a hard metal or oxide, pileup of oxide and polymeric contamination (particularly in the case of the platinum family of contact materials) and subsequent increased contact resistance and intermittent or total contact failure. Wear or cut-through of panel coatings and cable insulation can occur where contact occurs between insulated parts and sharp edges. Unbalanced cooling fans may be an inadvertent source of vibration.

Ultrasonically (U/S) enhanced cleaning systems have been found to cause fatigue failure of the wire bonds in open cavity integrated circuits where the resonant frequency of the wire spans is close to the frequency of the ultrasonic generator; this is probably not a cause of concern with solidly molded (non-cavity) components. The vibration (cavitation) of the cleaning liquid also results in erosion of the solder joints and fatigue of component external connections with high U/S energy densities. Fatigue and cracking of the joint or of the component termination appears likely only where the component termination system is mechanically resonant near the U/S generator frequency; solder joints to

LEDs and SOT-23 components appear to be more vulnerable than to other components, which is likely the result of the termination geometry. The thinner and more ductile copper SOIC leads appear to be more resistant to U/S induced fatigue than other terminations.

High energy repetitive assembly processes such as routing result in both in-plane and out-of-plane vibration modes in PWAs. In one case, accelerations on the order of 40-130 g's have been documented, with broken wire bonds, welded relay contacts, and broken crystal oscillator connections.

It is reported that gold plated relay contacts (such as those in reed relays) can suffer fretting corrosion during high frequency mechanical stress.

E-18.0 MECHANICAL OVERLOAD

Solder joints, initially good, are subjected to mechanical stress each time the assembly is flexed, shocked, or vibrated, for instance, TH component insertion, depaneling (by routing, shearing or scribe/break) or testing. Bending or flexing an SMT board after it is soldered puts severe stress on solder joints and components, as will the "straightening" of a warped board during insertion of the printed board into a cardguide. Board support/retention/clamping and vibration dampening during these operations, and printed board design aspects such as part orientation have been found to be techniques to minimize failed joints and terminations. One MLCC supplier, specifying a test condition of components mounted centrally on a coupon supported on 90 mm centers, requires that X7R and Z5U capacitors survive a 2 mm deflection and COG capacitors survive a 3 mm deflection.

A simple technique was developed to predict areas of high stress due to flexure influenced by rigid components. On a layout of the PWA, construction lines are drawn from the corners of the rigid components (such as connectors) and the construction line intersection defines the area of highest stress. Another area of high stress is the "fold-line" of an "L"-shaped printed board. TH laminated buss bars, TH radio frequency interference (RFI) fences and PGA packages are also in this "rigid component" category.

Failed solder joints and components adjacent to reworked components have occurred due to mechanical flexure and pressure stress during the component removal process.

Failed solder joints occur where connectors are assembled without mechanical restraints to minimize rotational or other movement of the connector relative to the printed board. These restraints could be springy (snap-in) detents (for wave soldering), rivets or screws (for hand soldering or possibly posts secured by heat-staking or ultrasonic deformation). Note that this is an order ranking from a Design For Assembly/Manufacturability (DfA/M) viewpoint.

E-19.0 EM SUSCEPTIBILITY, RADIATION, INTERFERENCE

If electromagnetic (EM) energy is induced in the traces associated with integrated circuits inputs or outputs, the results may be manifested as intermittent failure or secondary EOS. CMOS latchup may be initiated. The higher clock rates and faster transition times associated with the higher speed ICs can result in more EM energy generated and radiated from the product. The radiated energy may be gathered by other circuits or products and become an interfering signal. See also the literature on ESD, EMI, EM Control.

E-20.0 LOW ATMOSPHERIC PRESSURE/HIGH ALTITUDE/VACUUM

These stresses result in the expansion or explosion of gases in voids, resulting in overstressed sealed containers, packages and cavities (the "blowing" of liquid electrolytic capacitors vent plugs falls into this category); decreased air density and less efficient cooling (assemblies and systems may overheat, fuses with leaky seals will tend to open prematurely); decreased air density and decreased dielectric strength (initiation of corona, arcing and insulation breakdown with subsequent thermal and ozone damage as well as sprayed conductive materials, voltage breakdown and leakage in relays and connectors and other open [unsealed] conductors). "Sealed" cavity components may lose air and suffer the consequences of reduced gas dielectric strength.

E-21.0 IONIZING RADIATION

The most common source of ionizing radiation has been the outer package material (ceramic or plastic molding compound) of dynamic random access memories (DRAMs) where alpha particles are emitted by the heavy metals, such as uranium or thorium in the ceramic or oxide constituents; the alpha particles are absorbed by the storage elements of the DRAM and contribute electronic charge to the storage elements. This additional charge, on the order of one million hole-electron pairs per particle, can result in soft errors. Relatively thick layers of pure organic materials, such as polyimide, can "stop" the alpha particle from penetrating the silicon; unfortunately, these "stopping" layers can contribute to delamination of the molding compound from the surface of the protected die and subsequent corrosion.

Transient leakage currents and possible EOS can result if the energy of X-rays from a cathode ray tube is sufficient to penetrate the outer system package and the component package. See also CMOS Latchup.

Visible light is normally blocked by electronic component packaging; however, there are instances where light penetrates the packaging material, is absorbed in a semiconductor junction and contributes hole-electron pairs; optocouplers and photodetectors in plastic packages are

susceptible to light induced leakage, noise and malfunction.

E-22.0 SOLVENTS

Exposure of components and assemblies to various solvents (not normally considered a "stress") during assembly and repair operations can result in the following scenarios:

- loss of lubricant with subsequent accelerated wear, particularly in variable resistors and capacitors and in switches
- absorption and diffusion through polymeric seals with subsequent corrosion, particularly in aluminium capacitors when halogenated solvents, such as CFCs, have been used
- dissolution of some wire insulation "varnish," marking inks and label adhesives with subsequent contamination of the cleaning system, loss of the insulation function, or loss of identity
- dissolution or softening of plastics such as polycarbonate and polystyrene, even when low activity solvents such as CFCs have been used, solvation effects are exacerbated when solvent blends containing methylene chloride are used
- and absorption and deformation of silicone rubber parts and seals in CFCs.

Because CFC based solvents are being replaced by other solvents due to concern over ozone depleting effects, great care must be exercised in the replacement process. For instance, cleaning of SMT boards with a "plug in compatible" solvent prior to paste application has been found to greatly increase the frequency of "solder balls" apparently due to chemical reactions between the thermal decomposition products of the solvent and the tin in the solder during the soldering process. The composition, location and quantity of the residual contamination will also change with changes in the solvent.

The very high velocity solvent sprays used in the flux removal systems designed to achieve very clean PWAs particularly in SMT are intended to clean under and between components which are tightly fitted together. Marginal "O"-ring seals may succumb.

Appendix F
Components

Some SM component packages require special mention:

F-1.0 CERAMIC LEADLESS CHIP CARRIER (CLLCC)

Printed board material of high Tg and low CTE may be required to meet the reliability target.

F-2.0 METAL ELECTRODE FACE BONDED (MELFs)

Metal electrode face bonded (MELFs) require either special "U" shaped land patterns or adhesive to retain position during reflow.

F-3.0 SPACING ABOVE BOARD

The maximum height of printed board mounted devices must be considered during the planning stage of the design. Clearance restrictions may include the housing or enclosure proposed for the finished product or in the case of rack mounted printed boards, line-to-line clearance between components of one board and the surface of the parallel mounted assembly.

Assembly systems have clearance limitations as well. Most lower profile devices are mounted in the first stage of the assembly process with higher profile devices added at a later time. For excessively high profile devices, transformers and large connectors for example, post assembly attachment is required.

F-4.0 ALL SM PICK AND PLACE FEEDER PARTS

Sensitive or not, if they are dispensed adjacent to electrostatic discharge susceptible (ESDS) components, should be packaged in antistatic materials.

F-5.0 COMPONENTS WITH RUBBER SEALS

Should not be used with halogenated solvents or chemicals during production assembly, rework, field repair. This avoids internal corrosion caused when the halogens diffuse through the rubber seal. Aluminum electrolytic capacitors, when used, should be epoxy sealed. The rubber seal in rotary or slide components such as potentiometers and switches can deform or degrade under SM reflow temperatures. This seal can also allow intrusion of liquid during high pressure or high velocity spray cleaning.

F-6.0 PLASTIC SM COMPONENTS, MOISTURE, AND SM REFLOW PROCESSING

Plastic encapsulated surface mount components (PSMC) can suffer from thin film stress, delamination and cracks during SM reflow processing. These defects can lead to dendrites, thin film cracking (TFC), damaged bonds, bond pad cratering and corrosion, resulting in product failures due to opens and shorts of either a permanent or intermittent nature. The SM solder reflow process and, in some cases, the high junction temperatures associated with CMOS latch-up, causes absorbed moisture in the PSMCs to rapid convert to steam, causing the plastic to separate or delaminate from the die surface and inducing stress at this interface. During accelerated life testing under biased 85°C/85% RH conditions, one major computer maker noted a 50% decrease in MTBF on delaminated or cracked packages compared to defect free packages.

Similar failure mechanisms affecting PSMCs during SM reflow include voids and delamination resulting from the reflow and expansion of internal solder joints and expansion of coatings and potting compound, such as those found in networks of passive components such as capacitors, resistors, and delay lines. Also found in PSMCs are cracking and bursting of the outer plastic housing in components such as pulse transformers due to thermal expansion of the stress-relieving silicone conformal coating. These effects are in addition to any delamination of the silicone from the epoxy potting compound. The CTE of the silicone is on the order of 300 ppm/°C.

PSMC packages which contain integrated circuits (IC), resistor networks and capacitor networks are generally molded in an epoxy-based compound which contains silica and other fillers and additives which help control the coefficient of thermal expansion (CTE), adhesion of the molding compound (MC) to the various elements within the package (such as the leadframe, thick film substrate, and the IC chip), and the flexural modulus of the MC. When the thermosetting MC is cured, it shrinks and applies stress to the various elements in the package. This initial manufacturing-induced stress increases at cold temperatures. "Low stress" MC have been developed to address this issue. Delamination and internal cracking can also arise from this initial stress. During storage and transportation, particularly in ambients with high humidity, the plastic absorbs water vapor from the environment. The water vapor diffuses into the body of the package, "piling up" at impermeable interfaces such as the back of the die attach paddle, and the front of the IC chip. When the package is exposed to the 220°C+ temperatures of SM solder reflow or immersed in the 260°C wave solder, the water/vapor at the interface rapidly expands and tends to force the MC away from the interface.

If the adhesion of the MC is insufficient, the MC separates (delaminates) from the leadframe, substrate or chip. The extent of this separation may be partial or complete over the interface, and is generally observed to initiate at corners of the die attach paddle, at corners of the chip or lead fingers (tips of the interior ends of the leadframe leads to

which the bond wires are connected to complete the circuit from the IC bond pads).

The adhesion of the MC to the leadframe can be enhanced by topical application of coupling agents or adhesion promoters such as hexamethyldisilazane. If the strength of the MC is insufficient, this degradation process progresses to internal cracks in the MC, generally starting at sharp edges and corners of the various elements in the package. If the strength of the MC is inadequate, the cracks can progress in the worst case to emerge on the surface of the package. In milder cases, the cracks are internal and may terminate on the lead fingers. ANSI/IPC-SM-786 illustrates these progressive stages. Because stress concentration is known to be very strongly dependent upon the radius at the edges of the die attach paddle, a suggested crack reduction technique is to increase the radius at these edges.

Another result of moisture absorption by the plastic is an apparent decrease in the glass transition temperature (Tg) of the MC. This change in Tg means that the moist plastic expands and contracts more with changes in temperature due to soldering processes than when the package was initially manufactured. Because the CTE of the MC is much higher than the CTE of the chip, substrate or leadframe, the MC expands and contracts with respect to these other elements, introducing additional stress at the interface. This stress, in the case of ICs, can result in bond pad cratering and is additional to the stress caused by the initial IC package curing process. Moist PSMCs exposed to temperature cycling demonstrate a rapid progressive delamination and product failure; dry PSMCs exposed to the same T/C conditions show very slow progressive delamination. The conclusion is that vulnerable PSMCs can be robust to delamination under T/C if kept dry.

F-6.1 Shorts and Resistive Shorts in PSMCs

In common with through hole (TH) components, PSMCs suffer from metallic dendrites between the lead fingers and between leads. Dendrites are very thin, fragile metal "branches" which can be destroyed by casual contact or by currents on the order of several hundred microamperes. Dendrites form on surfaces and in cavities when the following conditions are present: continuous liquid water film thicker than several molecules; hydrolyzable, ionizable contaminant, particularly halides and acids, typically from solder flux but may also be extracted from the MC by the diffusing moisture; metallic conductors, particularly silver, copper, lead and tin (where halides are present, gold will also dendrite); electrical DC bias at low current levels between the conductors. See also IPC-TR-476A.

Liquid water films occur in the package (or on the printed board surface) when: the ambient humidity (relative humidity) is high; the exposure duration is sufficient to saturate the package (weeks to months at 25-35°C); there is delamination, cracking or voiding in the package due to initial manufacturing conditions or subsequent assembly operations; there is power dissipated in the package insufficient to keep the water in the vapor state.

Where the ambient temperature is suddenly reduced, we would expect that internal moisture vapor will condense at the interfacial voids. When cold parts are exposed to a humid environment, we expect superficial condensation.

Dendrites have been observed to be a result of: polyimide film delamination from the MC; voids in the MC due to improper material handling or due to improper process parameters during the molding process; cracks between lead fingers due to mechanical stresses applied during IC manufacturing processes such as trim/form and thermal shock stresses applied during IC manufacturing processes such as solder dip; cracks between lead fingers due to printed board assembly processes such as TH insertion and SM pick-and-place; delamination along lead fingers and leads which extend to the external surface of the package.

Cratering in silicone or GaAs ICs shows up under bonding pads as cracks due to stresses introduced by the wire bonding process. Cracks can grow during thermal shocks and temperature cycling, allow metals such as aluminum to move from the pad to the underlying semiconductor material, and are manifested as a resistive short from the bondpad to or through the underlying junction.

F-6.2 Opens and Intermittent Opens in PSMCs

Opens have been traced to wirebreaks where the MC is cracked, whether the crack originates from the chip, die attach paddle, or lead finger.

Predictions by finite element analysis and data from packaging stress test chips indicate the highest molding and thermo-mechanical stresses will occur at the corners of ICs and substrates.

Opens in metal conductors have been traced to stressed metal patterns (thin film cracking or TFC) in the corner of IC chips. Experiments with planarized passivation/metal patterns show metal damage when delamination is NOT seen. Experiments with non-planarized patterns show metal damage when delamination IS seen. Planarization of the passivation/metal patterns was introduced in ICs to minimize stresses transmitted to the patterns by the initial molding process. Minimized stresses are also the focus of the "low stress" holding compound formulations.

Corrosion and open metal conductors occur on IC chip surfaces when the passivation is stressed and ruptured and the package experiences the conditions described under "dendrites." Where the passivation structure includes a phosphorous pentoxide, P_2O_5, rich silicon oxide layer, a liquid water film can react with the P_2O_5, creating phosphoric acid, an excellent dissolver of the aluminum metal conductors. This effect has been mitigated by incorporating

boron trioxide, B_2O_3 into the silicone dioxide layer, forming a boro-phospho-silicate glass (BPSG).

Corrosion and opens occur on IC bond pads where the MC is delaminated, particularly in the corners of the chips in PSMC. Corrosion-related opens occur on any bondpads in TH packages where delamination, cracking or MC voiding has occurred, particularly on bonding pads associated with centrally located lead fingers.

Intermittent opens have been observed in PSM, as well as in PTH packages where the delamination or cracking occurs at the tip of the lead finger, causing wedge bond lift or wire break. Delamination can also occur at the ball bond/pad site. The separation of the wedge bond from the lead finger, the ball bond from the bond pad, or the broken wire ends from each other are microscopic. The separation may be very sensitive to changing temperature and is often intermittent. The product may fail during temperature ramps, but may be functional at the endpoint temperatures.

F-6.3 PSMC Delamination and Thermal Resistance ($_{jc}$ Degradation)

Delamination and debonding of the die attach paddle/heat spreader from the MC results in heat transfer by conduction through the gases in the voided region with an increase in the θ_{jc}. There is no data on the effect of various degrees of delamination/ debonding on the magnitude of θ_{jc}. Further the increase in θ_{jc} appears to be: greater for thinner packages; greater for packages of thermally conductive MC; expected to first appear in the corners of the die attach paddle; more significant for the package surface where heat is conducted to the printed board or to a heatsink by such means as thermally conductive adhesive; more significant for those components where heat dissipation or chip temperature uniformity is critical and where variations in these parameters affect performance or reliability.

F-7.0 RESISTORS

When resistors overheat or fail, the printed board underneath is often thermally degraded (with color changes in the laminate or coatings as well as decreases in resistivity of the laminate) or even charred, leading to catastrophic failure and smoke. The pyrolytically generated gases may or may not ignite. Printed board damage may be minimized by placing a copper pad under the resistor; the additional copper reduces the peak temperature experienced by the printed board during overload of the resistor.

Above the critical value of resistance (where maximum rated power is dissipated at maximum rated voltage), use voltage derating rather than power derating.

Through-hole (TH) resistors are generally spaced apart both because of their bulk and their need for PTH lands on the substrate. Surface mount (SM) resistors can be squeezed together because of their small size and because of the small surface area required for lands on the substrate. This opportunity for higher spatial density is rarely refused by the designer; the result is higher power density on the substrate.

TH and SM resistors dissipate their heat primarily through their leads, which are both electrically and thermally conductive, to the substrate conductors and thence to the air. Because of the reduced solder land area on the SMT substrate, the joint temperature will probably be higher in the SMT version of a TH product.

TH resistors have a relatively large surface area available to dissipate the heat to the air; in contrast, the active area of the SM device is relatively small. Inexpensive TH resistors are generally metal or carbon film. A relatively large volume or mass of material is available to dissipate both steady state and pulsating peak heat. Inexpensive SM resistors are generally thick film in nature and printed on one surface of a rectangular ceramic (generally alumina) body of low thermal conductivity.

The SM active element has a very small thermal mass; the active area of the SMT component can rapidly respond to increased power input with increased active element temperatures. Some resistor suppliers provide ratings on their product performance as a function of duration of stress at given temperatures and during assembly processing. SM resistor power dissipation ratings should be approached with caution; the data is generally obtained by the manufacturer in an undefined environment possibly described by a single resistor and an environmental chamber with moving air of unspecified velocity. Thermal finite element analysis (FEA) and IR scans are recommended for verification of hot spot location and magnitude. The presence of multiple heat dissipating elements in close proximity reduces the power dissipation allowable for any given element. No SM resistor manufacturer has provided allowable active film or component surface temperature data.

F-7.1 A Checklist for Power Resistors

- Locate resistors for favorable convection cooling.
- Provide mechanical clamping or thermoset heat transfer material to improve conductive heat transfer from power resistors to heat sink or chassis.
- Use short leads whenever possible so that traces and leads provide sufficient "heat dissipation" capability-unless physical distance from the printed board is required to minimize heat rise in the printed board.
- Individual power resistors over 10 cm long mounted with axis horizontal to minimize hotspots along length; average temperature of vertical and horizontal mounted resistors is about the same.
- Groups of power resistors mounted with axes vertical. Stagger resistors horizontally so that they don't direct hot airflows to their vertical neighbor.

- Design for a patch of copper foil beneath the body of axial power > 2 Watts resistors to minimize charring of the printed circuit board during fault conditions.
- At very high surface temperatures, radiation effects can be significant.

F-7.2 Trimmed Resistors The resistance value of rectangular or cylindrical, thick-film or thin-film resistors is adjusted by laser thermal ablation, sandblasting or abrasion. On cylindrical film resistors, high speed spiral grinding or abrasion is also used to adjust the resistance value. On some rectangular thin metal-film resistors, controlled oxidation of the metal is used to adjust the resistance value.

The mechanical abrasion or thermal ablation resistance value adjustment processes leave a narrow kerf. The kerf, if bridged by conductive materials such as flux, can be the site of surface leakage. The kerf can also be the site of voltage-induced breakdown, depending on the kerf geometry. See also voltage stress and moist environment notes. Note that the kerf on a TH Axial resistor which has been trimmed to value is generally quite long compared to the kerf on a rectangular SM device; hence the potential across the kerf of the TH component is lower (less stress) than that across the kerf of the SM component. In general, the kerf is mechanically protected from the environment by a plastic conformal coating. The kerf of any trimmed resistor is best protected by a glass or inorganic coating which covers the resistive and conductive areas; under conditions of severe thermal or mechanical stress, even the inorganic protective glaze can chip, crack or craze, leading to corrosion and failure of the resistive film or termination.

F-7.3 Fixed Resistors Use metal oxide above 1 Watt or wire-wound resistors above 2 Watts.

SM Metal Electrode Face bonded (MELFs) configuration components may require special "U–" shaped land patterns to reduce rolling or may require adhesive to retain position during reflow.

F-7.3.1 Metal Film Resistors Use for high stability, long life, high frequency, reliability and accuracy.

Metal-film resistors perform better in applications requiring precision and stability compared to wire-wound resistors according to warranty data.

Specific Cautions: Humidity or salt air can cause shunt paths on surface of resistor and shorting between spirals. Opens can be caused by mechanical damage. Higher noise than wire-wound. Spiral cut: Opens may occasionally occur due to too thin a resistance track due to non-uniform resistance spiral. Operation at RF above 100 MHz may produce inductive effects. Shorts may occasionally occur due to protuberances on adjacent resistance spiral. Operation at > 400 MHz results in reduced effective resistance due to dielectric effects. Critical matched resistors should be purchased and installed as a set. Resistive film can corrode if encapsulant or conformal coating is breached; a common point of entry for water or conductive contamination is the juncture of the terminal and overmoulding material or conformal coating. Mechanical stresses affect this type at temperatures < – 55°C.

Metal films of nickel-chrome (NiCr) alloy (aluminum doped) are susceptible to corrosion when exposed to halide compounds such as chloride-bearing fluxes if there is damage to the coating during component manufacture or printed board assembly, and subsequent exposure of the component to corrosive materials and moisture. The aluminum dopant is very sensitive to basic or halide solutions such as fluxes and saponifiers; the presence of this dopant should be identified for ease of failure analysis. This caution applies to TH as well as SM thin-film resistors, both epoxy coated and bare. Require your supplier of nickel-chromium (nichrome) resistors to identify use of aluminium as an alloying agent.

Small thin-film resistors of high value (> 100 kΩ) are the most susceptible to moisture.

F-7.3.2 Thick-Film Resistor Networks Good tracking between components on the same substrate.

Resistive film can corrode if encapsulant or conformal coating is breached. Mechanical stresses affect this type at temperatures < –55°C.

F-7.3.3 Metal Oxide Film Resistors Resistive film can corrode if encapsulant or conformal coating is breached. Mechanical stresses affect this type at temperatures less than –55°C.

F-7.3.4 Resistor Chips

Caution

General purpose SM resistors are generally thick-film cermet on ceramic substrate. Note the ESD sensitivity of bare films and metallic thin films over thin oxides. See also the comments on trimmed film resistors.

The reduced component lead surface area of SM resistors results in higher thermal resistance from resistive film to air. The smaller component and layout areas can result in higher power densities and hence higher resistive element temperatures. The smaller heat dissipation areas can result in higher solder joint and substrate temperatures. Avoid resistors that have been trimmed more than 50% of value.

Opens occur in the SM ceramic component body due to damage from mechanical stresses such as overload from vibration, shock or flexure of the PWA during service life.

Opens occur in the SM ceramic component body and in the body-to-termination interface due to damage from

mechanical stresses under post-soldering stresses such as twisting, flexing or shock and vibration during assembly operations such as TH component insertion, depaneling or testing. Identify the high stress areas of the printed board and avoid placing large, susceptible components in these areas. Minimize PWA flexure by providing adequate support and vibration damping in the fixturing.

Hard pick and place (P/P) tooling can cause mechanical shock during SM pick and place; test probes landing on SM component body or component terminations may also result in mechanical shock damage during testing. These tooling shock cracks generally occur in the middle of the component, although test probes can cause cracking and spalling at the impact site.

The EIA 1210 size should be an upper bound for reflow attachment of leadless ceramic and ferrite components to polymer-glass substrates; these components include leadless chip carriers (LCCs), multilayer ceramic capacitors (MLCCs), chip resistors, inductors and networks. At or above this size, compute a solder joint "Figure of Merit" to evaluate the impact of package size and lack of lead compliancy on solder joint reliability on glass-epoxy substrates. For specific guidelines, see Appendix A.

F-7.4 Variable Resistors Variable resistors (pots) have electrical and mechanical failure modes associated with the wiper in addition to all of the frailties ascribed to fixed resistors. The wiper contact resistance can vary due to wear, contamination or corrosion, wiper current, or vibration. The wiper position can shift due to shock or vibration, so that the wiper setting is affected by shipping or portable use. The current "rating" of the wiper is often an absolute maximum number which is guaranteed only to the extent that the resistor will not self destruct; the wiper current contributes noise voltage. The maximum power rating is based upon heat dissipation over the entire resistive element and is specified with "maximum resistance engaged."

Variable resistors require special precautions in manufacturing areas to avoid contamination by the soldering and cleaning processes. Sealed units require very tight process control by the supplier to survive the rigors of wave soldering, SM solder reflow processes and high pressure cleaning processes. If you must use variable components, hand-install (backload) the parts or process them sealed prior to and during soldering/cleaning. Avoid variable SMT components which have rubber or sliding seals around leads or shafts.

TH variable resistors generally experience soldering temperatures only on the terminations during wave solder. SM variable resistors experience high surface and internal component temperatures during solder reflow. Elastomers used in the seal area can be degraded by this heat exposure. The thermoplastics used in the housing and rotor can see very high surface temperatures during solder reflow processing. A small change in the nominal dimensions of an "O"-ring was found to lead to the ingress of flux into a sealed pot. The supplier's "standard" bubble test was found to be inadequate to detect the problem before the problem was found after assembly.

If halogenated solvents, activated fluxes or saponifiers leak past the seal, enter the component cavity, dissociate and are then exposed to moisture, one result is lowered insulation resistance. If there is electrical bias present, we have seen migration of the thick film electrodes (generally of silver) and shorting. Metal migration tracks (dendrites) are very fragile; the "short" can disappear with minimum mechanical movements and may be noted as an "NTF." A change in flux application method on a wave soldering machine was found to be responsible for the ingress of flux into a sealed pot.

Silver dendrite growth has been observed inside potentiometers due to intrusion of high pressure wash water past improper, cracked or heat-distorted seals.

F-7.4.1 Enhancing Variable Resistor Reliability

1. Do not use a variable resistor, if possible; replace rotating or sliding variable resistors with solid state switches and programmable resistors. Elimination of a component which requires adjustment on test is a DfM guideline.

IF YOU MUST USE A VARIABLE RESISTOR,

2. Minimize the effects of contact resistance variations on performance; use the wiper in a potentiometer mode; draw low current through the wiper- but too low wiper current can also cause problems.
3. Minimize the effects of contact resistance variations on performance; incorporate a low pass filter capacitor after the wiper to minimize noise voltages.
4. Count on no more than 1 degree of arc (0.3%) resolution with a 1-turn pot. Don't expect infinite wiper position resolution or perfect stability.
5. Consider the maximum current specification as well as the maximum power specification.
6. Use sealed variable resistor components where the value must be varied by hardware means and where the component must survive an inline cleaning process.
7. Pay close attention to the control exercised by the supplier on raw materials and process, particularly on items such as rubber seals and their associated dimensions.
8. Hand load variable components as necessary to enhance the reliability of your PWA.
9. Be sensitive to "NTF" in returns.

Caution

All variable resistors can suffer movement of the wiper on the resistance element as the result of shock or vibration. In critical applications the resultant change in output voltage can constitute a "failure" of the resistor. Non WW units become noisier with wear life and will suffer resistance change due to humidity. Power ratings for all variable resistors are based upon the engagement of the maximum resistance by the wiper. Excessive currents can be drawn when less than maximum resistance is engaged, resulting in a burn out of the resistance element. Some pots use silver thick-film conductors; dendrites and shorts can form if water leaks past the "O"-ring seal during cleaning.

F-8.0 CAPACITORS

Capacitors suffer from high frequency and high voltage effects of sinusoids; performance characteristics derived at low frequency may not extrapolate to higher frequency; the same is true for characteristics obtained at low voltage.

F-8.1 Multilayer Ceramic Chip Capacitors

Caution

Keep the MLCC termination electrodes $\Delta T/\Delta t < 4°C/$ second and ΔT of < 100°C from preheat to peak body temperature under SM reflow, wave solder and hand solder process conditions to avoid cracking of the internal dielectric layers. Components with the highest values of dielectric constant and largest numbers of dielectric layers are most susceptible to thermal shock and impact stresses. Shorts occur due to silver electrode metal and end termination metallization migration under temperature/ humidity/ bias stress. Reducing the volume of the solder fillets or narrowing the pad sizes to less than the component lead width.

Opens occur in the component body due to damage from mechanical stresses such as overload due to vibration, shock or flexure of the PWA during service life.

Opens occur in the component body and in the body-to-termination interface due to damage from mechanical stresses under post-soldering stresses such as twisting, flexing or shock and vibration during assembly operations such as TH component insertion, depaneling or testing. Identify the high stress areas of the printed board and avoid placing large susceptible components in these areas. Minimize PWA flexure by providing adequate support and vibration damping in the fixturing.

Hard pick and place tooling can cause mechanical shock during SM pick and place; test probes landing on component body or component terminations may also result in mechanical shock damage during testing. These tooling shock cracks generally occur in the middle of the component, although test probes can cause cracking and spalling at the impact site.

The EIA 1210 size should be an upper bound for reflow attachment of leadless ceramic and ferrite components to polymer-glass substrates; these components include leadless chip carriers (LCCs), multilayer ceramic capacitors (MLCCs), chip resistors, inductors and networks. At or above this size, compute a solder joint "Figure of Merit" to evaluate the impact of package size and lack of lead compliancy on solder joint reliability on glass-epoxy substrates. For specific guidelines, see Appendix A.

TH versions of MLCC (disc caps; dipped rectangular; axial leaded ceramic) may demonstrate weakening of internal low temperature solder connections due to assembly soldering heat.

Be wary of suppliers of "precision" MLCC based components who adjust the value of their part by abrading or otherwise removing dielectric and conductor material; the commonly used plastic coating is not a reliable replacement for the original ceramic layers and silver migration is likely. In "hi-k" capacitors, dissipation factor and dielectric constant are affected by DC voltage, AC voltage, and temperature.

For conductive adhesive attachments to SM components, do not use nickel, tin and lead for final component termination finishes; the oxides of these metals are not conductive. Oxygen and water can diffuse through epoxy and oxidize the underlying component termination finish. The initial ESR of nickel terminated MLCC capacitors is higher when epoxied than when soldered; the Q factor is lower for epoxied devices. The increase in ESR of these MLCC capacitors was also significantly higher after aging at 100°C/100% RH for 4 hours or at 155°C for 16 hours. Epoxy cure temperatures higher than the melting point of tin-lead solder will cause the solder to flow away from the cured epoxy interface. Epoxies are expected to be more elastic compared to solder, but −55/+125°C temperature cycles with 10 minute dwells showed similar fatigue curves out to 100 and 1000 cycles for both epoxied and soldered capacitors. Silver oxide is conductive and gold and palladium do not tarnish or oxidize; use silver and these noble metals, historically used for hybrid component termination finishes.

F-8.2 Plastic Film Capacitors Excess body temperatures during SM reflow will result in dielectric film softening and dielectric film thinning with:

- loss in voltage capability
- increase in capacitance and leakage current
- increase in intermittent or permanent shorts
- increase in ESR may increase

In the extreme case, the result may be intermittent internal solder joints.

F-8.3 Solid Tantalum Capacitors Tantalum solid electrolytics are preferred to aluminum electrolytics for stability and reliability.

Caution

Excessive assembly soldering heat results in solder melting and solder balls at internal connections. Some devices are available in plastic encapsulation to limit internal heat absorption during SM reflow.

Be aware of undamped reflections of switching transients due to the parallel capacitance/series inductance geometry on the power/ground distribution net of many PWAs. Visualize the resemblance to the ideal configuration for a delay line with series inductors and high quality parallel capacitors in the schematic and layout of SMT PWAs; the long power and ground conductors contribute the series inductance and high Q multilayer ceramic capacitors between power and ground provide the parallel capacitance. At low temperatures, silicon mobility increases and therefore decreases the time rate of change of switching transients; the edges get faster. Lossy electrolytic capacitors may have to be applied between power and ground to dampen the reflection of those switching transients.

Limitations include relatively high leakage current; voltage range limited to 6 to 120 V. Only available polarized and polarity must be observed; where handload or repair is expected, mark the printed board to facilitate correct insertion- this is also a DfM guideline.

Self healing effect of high leakage current on MnO_2 results in lower incidence of shorts due to dielectric breakdown but must use 3Ω/V current limiting resistor.

Opens due to poor solder or weld internal connections which are damaged during vibration or shock.

F-8.4 Electrolytic Aluminum Capacitors Use where large values are required and excess capacitance is allowable.

Caution

Low air pressure accelerates loss of electrolyte.

High body temperatures result in boiling of electrolyte, loss of capacitance, increase in equivalent series resistance (ESR), and spillage of possibly corrosive electrolyte. Some styles are available in plastic encapsulation to prevent electrolyte loss.

Storage at room or high temperature results in drying out of electrolyte or corrosion of case. During storage, aluminum oxide dielectric electrochemically combines with electrolyte and capacitance value decreases; connection between electrode and aluminum dissolves in electrolyte and opens. Operation at very severe derating conditions also allows the aluminum oxides to "reform" and the resulting capacitor is lower in voltage capability.

Low temperature can cause freezing of electrolyte.

Vacpk + DC < rated working voltage. Vacpk < DC Voltage. No reverse voltage.

Rubber or elastomer seals cannot halt the ingress of common SMT cleaning halogenated solvents (and previously after TH wavesoldering using the synthetic activated flux/ Chlorofluoro-carbon cleaning combination). Rubber seal degrades in halogenated solvent wash- the solvent is catalytically degraded by the aluminum and the degradation products include HCl. The HCl dissolves aluminium. This halide corrosion is a major constraint on rework. Where this kind of corrosion has occurred in OEM product, any component cost savings were lost in the expense of the recall, rework and repair of the product. Rubber-sealed aluminum electrolytics must be used in conjunction with non-halogenated solvents, non-halogenated chemicals or water wash to avoid the introduction of corrosives during manufacturing and factory rework or field repair.

There are plastic encapsulated SM and TH versions of rubber-sealed capacitors which seal out halides and seal in dielectric fluid.

Some aluminum electrolytics use the polar solvent dimethyl-formamide (DMF)- a suspected carcinogen and a solvent for and degrader of solder masks and epoxy conformal coatings. Better for environmental health and safety purposes are aluminum electrolytic fluids of gamma butyrolactone (GBL) or dimethyl acetamide which are also polar solvents. Leaking polar electrolyte drastically reduces the SIR of the PWA. Orient vent plugs of electrolytic capacitors to minimize damage consequent to component failure; face vent plugs away from substrate.

Reverse voltage results in burn out and opens.

F-8.5 Variable Capacitors Do not use variable capacitors, if possible.

Caution

For greater stability, use air trimmer. Variable capacitors require special precautions in manufacturing areas to avoid contamination by the soldering and cleaning processes. Sealed units require very tight process control by the supplier to survive the rigors of wave soldering, SM solder reflow processes and high pressure cleaning processes. If you must use variable components, hand-install (backload) the parts or process them sealed prior to and during soldering/cleaning. Avoid variable SMT components which have rubber or sliding seals around leads or shafts.

F-8.5.1 Variable Piston Capacitors Designs vary in temperature stability.

Caution

Shorts due to contaminants within capacitor such as thread wear debris or gold plating shaken loose by vibration. Opens due to internal solder connections rupturing during assembly solder operation.

F-9.0 INDUCTOR/TRANSFORMERS

Caution

Operation at less than rated lower frequency may result in overheating and loss of inductance.

Multilayer SM ceramic and ferrite inductors (and filters) are susceptible to soldering process thermal shock. Limit the termination electrodes $\Delta T/\Delta t$ to less than 4°C/second and ΔT to less than 100°C from preheat to peak body temperature under SM reflow, wave solder and hand solder process conditions to avoid cracking of the internal layers. Components with the largest numbers of ferrite layers are most susceptible to thermal shock and impact stresses.

Do not subject internal connections of encapsulated components to assembly solder process temperatures > melting point of specific solder alloys used; skip this caution if the connections are welded.

Opens occur in the component body due to damage from mechanical stresses such as overload due to vibration, shock or flexure of the PWA during service life.

Opens occur in the component body and in the body-to-termination interface due to damage from mechanical stresses under post-soldering stresses such as twisting, flexing or shock and vibration during assembly operations such as TH component insertion, depaneling or testing. Identify the high stress areas of the printed board and avoid placing large, susceptible components in these areas. Minimize PWA flexure by providing adequate support and vibration damping in the fixturing.

Hard pick and place tooling can cause mechanical shock during SM pick and place; test probes landing on component body or component terminations may also result in mechanical shock damage during testing. These tooling shock cracks generally occur in the middle of the component, although test probes can cause cracking and spalling at the impact site.

The EIA 1210 size should be an upper bound for reflow attachment of leadless ceramic and ferrite components to polymer-glass substrates; these components include leadless chip carriers (LCCs), multilayer ceramic capacitors (MLCCs), chip resistors, inductors and networks. At or above this size, estimate solder joint reliability to evaluate the impact of package size and lack of lead compliancy on solder joint reliability on glass-epoxy substrates. For specific guidelines, see Appendix A.

Provide conductive heat transfer paths for these devices and locate for favorable convection cooling.

Delay lines may be constructed of purely passive components such as capacitors and inductors or may contain additional, active gain elements for impedance transformation and independence from loading variations. Silicone rubber is used as a conformal coating for protecting or relieving the wires and core in transformers and delay lines from molding stresses. The silicone with a high CTE of 200-300 ppm/°C will expand within its plastic enclosure during reflow and stress the enclosure. If there is too much potting compound or the enclosure wall is thin or weak, the wall will fail and allow moisture to enter the package and corrosion to start. The walls of the smaller SMT parts are thinner than their TH counterparts and the higher body temperatures during SM reflow make this phenomenon more likely to occur than with TH processing. Subsequent intrusion of moisture and ionizable contaminants into the component has resulted in dendritic growth and functional failures.

F-10.0 SEMICONDUCTORS

- Metallurgically (eutectic) chip bonded devices preferred but not feasible on very large die; hermetically sealed devices preferred for humid or corrosive atmospheres but generally costly.
- Devices with long, unsupported bond wires are more susceptible to vibration and shock.
- Brazed terminations may employ combinations of metals which, if exposed at edges and cracks, can result in galvanic corrosion under humid conditions.
- Packages such as SOT-23, with a metallic leadframe comprising a high percentage of the plane area, demonstrate an effective X-Y CTE closer to that of the leadframe material than of the encapsulating plastic.
- SM metal electrode face bonded (MELFs) configuration components may require special "U"-shaped land patterns to reduce rolling or may require adhesive to retain position during reflow.

F-10.1 Light Emitting Semiconductor Diode (LED)

Caution

Packaging must be characterized to perform under the conditions of your soldering and cleaning operations; LEDs which exceed the 105-125°C glass transition temperature (T_g) of the plastic body when immersed in wave solder and experience delamination of the plastic from the leadframe. If you must wave solder these components, observe the cautions for very moisture sensitive PSMCs. Some plastic encapsulated LEDs are susceptible to thermo-mechanical stress from the encapsulant at very low temperatures. LEDs with shallow junctions or small area junctions may be susceptible to ESD. Proper current limiting or regulation must be provided to observe average current guidelines. Peak current "on" periods < time constants of the chip in package.

F-10.2 Digital Semiconductors

Caution

Where possible, obtain devices with BIT capability to ease testability requirements.

F-10.3 Digital Silicon Semiconductors (MOS MSI/LSI)

Not specified for most CMOS components (but should be requested), is the allowed or preferred turn-on sequence of power supplies, clocks, data and output loads. An improper turn-on sequence may result in latchup and subsequent damage to the chip.

F-10.4 Linear Semiconductors

Caution

Be aware of ESD vulnerability on high frequency/low current devices- get evaluation data; with supply below .8X nominal, device may be beyond recommended operation range. Plastic cracking issues discussed in Appendix E, particularly those associated with leakage currents, apply to linear ICs.

F-11.0 OTHER COMPONENTS

F-11.1 Fuse

Caution

Fuse elements in SMT versions have less heat dissipating capability (because there are no fuse clips) than otherwise identical TH versions and may require additional temperature derating.

F-11.2 Separable Contacts (Relays, Switches, Connectors, Sockets)

Caution

Condensation and contaminants on the printed board, flex circuit or wiring to the contacts can lower the insulation resistance between the contacts; the same result is obtained if the glass envelope of a reed capsule is contaminated. SM relays, switches, connectors and sockets in high impedance applications may require backloading during SM processing.

Non-sealed components should be backloaded. "Sealed" components should be evaluated for the robustness of the seal to SM cleaning factors such as solvents, water, high temperature, high pressure/velocity.

Intermittent open circuits in slide switches have been found due to washing out of contact lubricant during board cleaning with high pressure/velocity sprays intended to clean under components with very small clearances.

For environments with anticipated vibration or thermomechanical movements due to temperature cycling, contacts must be prevented from micromotion (displacements < 2.5 μm) during the manufacturing cycle as well as in the service environment:

- Sealed or uncontaminated soft metal contact finishes, such as gold, may weld under micromotion conditions (as well as under severe shock and vibration conditions such as SM panel routing or shearing).
- Volatile silicones are degraded in the contact area of open contacts under micromotion conditions as well as in the presence of electrical arcing; silicas and varnish buildup result in intermittent as well as permanent contact failure. This consideration may limit the choice of silicones in such diverse areas as solder masking tapes, adhesives, and resins to the non-outgassing types.
- Open contacts with contact finishes from the active catalyst platinum family, including gold may, in the presence of micromotion and condensible organic vapors, form insulating polymers; this consideration may dictate the choice of printed board, solder mask, flux, fluxing oils (under the conditions of SM processing) and conformal coating (under service conditions). With these catalytic metal contact finishes, non-outgassing plastics are required for switch and relay housings.
- Components of plastic materials susceptible to blistering at temperatures > 200°C must be dry (baked out) prior to SM reflow.
- After a soldering operation, assure that the component housing, contacts and printed board are not in a stressed condition; this stress-free condition is difficult to achieve with in-line SM reflow processing.
- Service environment parameters such as humidity, temperature, corrosivity must be known and accounted for. These factors determine material choices, contact configuration and housing configuration for robustness and protection from the environment.
- Do not use the same connector or switch contact pair for power and for "dry" or low power/low voltage circuit connections.
- ESD susceptibility evaluation of the assembly may be required if a switch or connector is accessed by the user; isolation of the circuit by plastic parts, air gaps or grounded shields and shrouds may be required.
- Do not "repair" stuck (welded) reed contact capsules by hitting them. Rhodium plating on reed contacts serves to control long term contact resistance and contact noise.
- Sheared edges of contact blades may be sites for galvanic corrosion.
- Do not derate "dry" contacts (low voltage, low current, low power); some electrical energy is required to break down oxide films. Gold or other noble metal

may be required for "dry" circuits with 0.1-5.0 V and 1- 10mA.

- Contact final finish material/underplate/thickness/porosity/smoothness is appropriate to the use environment, including frequency of reconnections and current-voltage conditions.
- Identify and avoid exposed galvanic couples such as terminations of copper-nickel-gold which are sheared after plating; in addition, exposed base metals on the edges of contacts can lead to tarnish creep, the extension of corrosion products of copper over the gold. See a sample galvanic compatibility table in the appendices.
- Suppliers' data usually arises from margin-testing which may not be long enough in duration under stress to make meaningful comparisons or judgments of performance in service; no failures under accelerated conditions means no data with respect to mean time to failure or with respect to scatter have been obtained.

Minimize fretting corrosion:

- Assure that only compatible contact finish combinations are used, such as gold-gold, with per-contact normal forces of 30-50 grams-force.

  Non-noble metal finishes require the availability at the contact interface of high current, high voltage or high energy to break down any developed oxides and other corrosion products; these conditions are not generally available with ICs which operate at required higher per-contact normal forces, e.g. contact mating finishes of tin to tin or tin-lead to tin-lead: < 200 grams-force initially and < 100 grams-force at end of life.
- Do not use incompatible contact finish combinations such as gold-tin.

  Under micromotion conditions arising from mechanical or thermo-mechanical causes, gold-tin intermetallic compounds are generated. These IMCs are high in resistance and result in intermittent or permanent resistive or opens connections.
- Investigate and satisfy any need for contact lubricants.

  With non-noble contact finishes such as tin or tin-lead, the environmental circumstances may indicate a possible need for oxygen/corrodant exclusion techniques such as the use of "lubricants;" lubricants are not preferred because they hold dust particles, may slowly evaporate or oxidize, and require special attention during service/replacement.
- Card mounting stresses and flex circuit flexures (static or dynamic vibration) must be controlled by clamps, screws, hold-downs; the stresses must not be transmitted to the connector or to the contacts.

F-11.2.1 Batteries Keep in a suitable, insulated or original container, not loose, in inventory, on the line and at repair stations. Otherwise, shorts may result in extremely high temperatures in the storage container. Use a battery holder designed with very high pressure contacts. To avoid the effects of fretting corrosion, do not interface dissimilar metals such as nickel and tin at the contacts. Welded connections are preferred for high vibration environments.

Liquid or gel electrolyte may boil or expand at SM reflow temperatures.

F-11.2.2 Separable Electrical Interconnections Separable SM interconnections include randomly laid plated wire bundles in holes in a hard insulative substrate (fuzz buttons); stamped and plated preformed springy material in an elastomeric matrix; stamped and plated preformed spring material in an injection molded connector housing; strips of metal film over an elastomeric core; plated etched or stamped metal films on an insulative flexible substrate, mated under pressure from an additional mechanical part; metal particles dispersed in an insulating polymeric matrix; or carbon or silver particles dispersed in a polymeric matrix and separated from each other by insulative polymeric material. The stamped/plated preformed spring mechanisms appear to afford a "wiping" action which scrubs tarnish from the mating surfaces. The silver plated contact materials may lead to dendriting with moist corrosive environments in combination with low powered circuits, if the elastomer does not form a gas-tight seal.

For reliability, the contact materials should be of noble metals and, in particular, no gold-tin contacts should be employed due to the formation of resistive gold-tin intermetallics under fretting corrosion conditions. Use caution with tin-tin or tin-lead contacts and specify contact normal force > 100 grams (force) per contact at end of life. Mechanical restraint of the mating parts to reduce micromotion to < 2.5 µm is recommended.

- Identify mechanical stress levels in metals (particularly formed terminations) which might contribute to stress corrosion or plating discontinuities; alternatively, form metals in the annealed state and post-plate.
- Verify that the operating temperature rating applies to the mated connector under the required combination of current/voltage/impedance. Where the required normal contact force depends in part on the plastic housing, that normal contact force may decrease with exposure at high temperature during assembly or service.
- Current rating per connector pin applies to the as-stuffed condition; the heat rise per pin must be accounted for in high current (paralleled power supply) situations.
- Evaluate each SM connector and socket style for inspectability of the solder joints as well as repairability. In many cases, the invisible socket solder

joints are expected to withstand very high IC extraction forces, both tensile and torsional, particularly if the extraction is performed with improper tools or technique. Similarly not-recommended components are TH sockets for SMT components.

Connector Mechanically restrain SM connectors to resist expected tensile, torsional, shear forces in service, repair and to resist lifting forces in assembly operations. Long connectors may result in warp of the PWA due to CTE mismatch effects during SM reflow and cooldown.

- Surface mounted sockets for SMT components may be considered a special purpose connector and should not be used except under specific circumstances which include the normal connector concerns AND:
- simulation of the effects of increased thermal resistance from the component case and junction to air (θ_{ja}) and (θ_{ca}) have yielded acceptable performance and Tj results,

  If your design can tolerate the increased θ_{ja} and θ_{ca}, then-
- Simulate the effects of increased electronic parasitics such as parallel lead capacitance and series lead inductance and verify acceptable high frequency performance. Watch for the effect of the added parasitics at every lead on such parameters as ground bounce, clock signal skew, and edge degradation; higher power dissipation is often associated with higher clock rates and faster switching times.
- No socket manufacturer warrants compatibility between gold component termination finish and tin or tin-lead plated socket contacts. Major socket manufacturers strongly discourage the use of gold socket contacts with tin or tin-lead component lead finishes because the socket systems for gold finishes are designed for much lower per-contact normal force. In either case, the concern is with the generation of high resistance gold-tin IMCs rather than the generation of corrosion products.

F-12.0 PRINTED BOARD

Caution

- SM printed boards are generally denser and may require additional thickness or stiffeners for stiffness during processing/testing/handling to avoid flexure and damage to solder joints and component bodies.
- Provide "balanced design" with similar areas of copper on each side of the board (around the neutral axis) particularly if, on one side of the printed board, MLCC bridge from a large ground plane to a large power plane.
- With ceramic components on FR-4 boards, accelerated stress testing which exceeds the glass transition temperature (Tg) of the board results in unreasonable, decreasing failure rates of the solder joint because the board material becomes more rubbery and less stress is introduced into the joint; this was found in research in the Mantech program at Martin Marietta.

F-12.1 Printed Board PTH/Vias

See Appendix B for details.

Identify risk sites threatening PTV reliability, such as:

- large environmental or power cycling temperature excursions
- small diameter vias or PTHs
- thick board
- low T_g board material
- high Z-axis CTE board material
- copper plating of low ductility and thin or non-uniform thickness
- aspect ratio (board thickness to barrel diameter) > 3:1

  Blind and buried vias, by their geometry, have a lower AR; a series of these vias are more robust to thermal stresses than a PTH with a high aspect ratio.
- Plated-through Vias (PTV) associated with through-hole components (such as connectors or pin-grid arrays) fail open at the knee after rework due to leaching or dissolution of the copper during long term exposure to molten solder (fountain or drag) during rework. See publications from the Tin Information Center (International Tin Research Institute) for the effect of temperature on dissolution rate of copper and for the protective nature of nickel plated barrier metal.

PTH thermal cycling failure risk reduction techniques include use of minimum diameter vias and PTHs only where needed, plating the barrel with nickel for reinforcement, use of higher T_g resin, additional innerlayer pads where possible to spread barrel stress, use of 2 ounce copper innerlayers to increase anchoring of barrel. See also IPC-TR-579 and section 4.7 in this design guideline.

- Tent all PTVs, if using active water soluble flux (paste or liquid), on both ends; alternatively, do not terminate open vias and PTHs under a component with tight clearance. A third alternative is to fill the vias and PTHs with solder, epoxy or modified solder mask/ conformal coating material. These techniques minimize barrel corrosion due to flux entrapment and avoid test fixture corrosion and loss if SIR due to drips of liquid flux.
- Require supplier data to confirm ability of PTV and vias to meet your realistic environmental test requirement for temperature extremes; temperature transition times; number of temperature cycles. Performance

specifications (PTV T/S, Solder Resistance, IPC-SM-840, etc.) should be defined with agreed upon test methods for evaluation.

F-12.2 Printed Board Conductor Design

- Only as needed, use minimum spacings from conductors to (conductor, mounting hole, component terminals) and from barrels to inner plane conductors and other barrels
- Minimize electromigration stresses by minimizing temperature and current density/current crowding:
- Use conductor widths adequate to limit $\Delta T_{conductor}$ less than 5°C.
- Use rounded corners
- Use minimum number of sharp/acute angles
- Use smooth transition fillets
- (With the above techniques, conductor cracking, foil lifting, voltage breakdown are also improved)
- Use metal deposition techniques which result in large, ductile grains
- Selectively plate pressure contact areas for reliable electrical contact to avoid "fretting" corrosion; e.g. gold to gold or tin to tin but not gold to tin. Gold which is pore-free and ~0.6 μm is required for pressure connections capable of "many" disconnects and for SM boards, may require selective gold plating. A nickel underplate of ~2 μm is required to prevent diffusion of copper into the gold.
- Subdivide large copper areas on the surface to prevent blistering/solder thieving
- Widen conductors which function as heat dissipators

F-12.3 Solder Joints

See section 4.6 and Appendix A for details.

Identify risk sites for solder joint non-reliability factors such as:

- Large $\Delta\alpha$ between component and substrate, particularly for ceramic components on FR-4 substrate or plastic components on ceramic substrate.
- Large components on any edge
- Non-compliant leads (short and stubby)
- Large ΔT in the use environment under power cycling conditions
- Thin solder joints
- Solder joints containing gold > 3 weight percent

  Gold thickness is more critical in SM than in TH because the volume of solder is limited to that of the paste "brick" and the gold content in the final SM joint is not as dilute as in the TH joint.

  Use printed board gold plating finish 0.1 μm on printed board surfaces to be SM soldered so that gold concentration is < 3 weight percent in the final joint to avoid significant solder joint embrittlement. See the note above on gold thickness required to assure reliable pressure connections.

  Dipping of the component leads in molten solder to dissolve and remove the thick gold is one historical method of "converting" gold plate part finishes to a safe termination finish; the resulting "solder dip" finish thickness is not uniform and may interfere with the formation of uniform solder joints.

- Solder joints to terminations finishes containing silver

  Joints to components can fail immediately if the terminations are manufactured with a final terminal finish of silver paste or palladium-silver paste; these materials rapidly leach into molten lead-tin solder and the resulting joint is weak. Avoid leaching by requiring a barrier metal layer of nickel over the silver for SM component termination. Thin silver or palladium plating over the nickel barrier is acceptable; the small amounts of Intermetallic Compound (IMC) formed are not detrimental.

  Alternatives required to allow silver in the manufacturing process and which result in reliable joints are

  — expensive in terms of hand labor, special processing or special materials

  — use special silver-bearing solders in production, rework and field repair

  — limit exposure of the solder joint to solder temperature

  — limit volume of lead-tin solder in the joint; this alternative may result in reducing solder attachment cyclic fatigue life.

- Solder joints to final terminations finish of nickel.

  Nickel metallization as a final termination finish results in highly variable solderability or poor solder joint yields if an aggressive flux is not used in SM reflow. Nickel is rapidly passivated (covered by a hard, tenacious, non-solderable oxide). In their journal, Siemens has reported the use of selective nickel plating on TAB leads to limit the spread of solder. The consequences of using a nickel termination finish may be extensive (uncontrolled) hand soldering to obtain satisfactory metallurgical joints at the cost of degrading component reliability.

  Strikes of porosity-free palladium or gold, on the order of 0.1-0.2 μm, can preserve the solderability of the nickel; silver plate on the order of 20-40 μm and tin or tin-lead on the order of 400-100 μm are also used for this purpose.

- Estimate solder joint reliability (see Appendix A).
- Solder joint risk reduction techniques include increasing the solder joint height, adding compliant leads, or

changing the materials of joint height, adding compliant leads, or changing the materials of substrate or component to decrease the $\Delta\alpha$.

- Perform DfM review of printed board layout- include ease of inspection and rework of all solder joints, particularly those adjacent to "tall" components such as connectors or in the PWA "valley" between such components. Placing the non-termination portion of the SMT component next to the TH component eases inspection. Packages with heatsinks overhanging the package edge lack inspectability and have a thermal shadowing effect on neighboring parts during reflow; a "shadowed" part may require removal of the heatsinked part for rework.

Appendix G
Coefficient of Thermal Expansion

G-1.0 COEFFICIENT OF THERMAL EXPANSION

Polymer systems expand with increasing temperature, demonstrating a glassy phase response with a coefficient of thermal expansion (CTE) or α_1 below T_g, and a rubbery phase response with a much higher α_2, typically 3 times α_1 above T_g. The transition from glassy phase to rubbery phase is gradual, but for most polymer substrates may be characterized by T_g, the glass transition temperature. See IPC-T-50.

Glass fiber reinforced substrates exhibit significantly different CTE in the z (CTE(z), out of plane) axis compared to the CTE in the x-y axes; for example, below its T_g, Quartz/Bismaleimide material with 35% resin by weight exhibits a CTE(x,y) of 6 ppm/°C and a CTE(z) of 41. Woven glass fiber reinforcement exhibits an additional difference between x and y axes on the order of 1-5 ppm/°C; this difference may be significant where the CTE of a large SM component package is to be matched to the CTE of the substrate to enhance cyclic life of the solder attachments.

The CTE(z) is particularly significant in determining the cyclic life of PTH and vias in SM PWAs because the aspect ratio (ratio of substrate thickness to finished hole diameter) is generally much larger than the corresponding aspect ratio achieved in printed boards manufactured for through hole technologies. Higher CTE(z) values result in higher cyclic tensile stress in the barrel of the PTH or via during temperature excursion during SM reflow, or SM component removal/rework/repair as well as during printed board fabrication, solder dipping, hot air leveling, or wave solder. See IPC-TR-579 and IPC-SM-782.

The thermal cycle reliability, vibration robustness, and the thermal management of high performance Surface Mount (SM) products are heavily dependent upon the constraining core such as Copper-Molybdenum-Copper (CMC), Copper-Invar-Copper (CIC) and Molybdenum-Graphite-Molybdenum (MGM) composite material systems.

The ratios of the various materials in those composite systems can be adjusted to tailor the effective CTE to the optimum value. The tradeoffs include weight and cost. See IPC-MC-324.

G-2.0 CONSTRAINING CORES

A constraining core is an internal supporting plane in a packaging and interconnecting structure, used to alter the coefficient of thermal expansion of printed boards.

Table G-1 Typical Values for Coefficients of Thermal Expansion (ppm/°C)

Insulator/Substrate Material/System	CTE lower	value	upper
E glass		5.5	
S Glass		2.6	
Glass-Ceramic		> 3.0	
Silicon	2.6		
Diamond		0.9	
Aluminum Nitride		4.5	
Silicon Nitride		3.7	
Quartz, fused silica	0.5		0.6
Kevlar 49		-5	
Beryllia	6		
Cubic Boron Nitride			
x-y		3.7	
z		7.2	
E Glass/Epoxy			
x-y	14.2		17.3
x	80		90
E Glass/Polyimide			
x-y	12		16
z		6	
E Glass/PTFE			
x-y		24	
z		260	
Kevlar/Epoxy			
x-y	5.1		7.1
z	5.1		7.1
Kevlar/Polyimide			
x-y	3.4		6.7
z		83	
Quartz/Polyimide			
x-y	5.0		8.0
z		68.4	
Quartz/Bismaleimide			
x-y, 35% Resin	6.2		6.3
z, 35% Resin		41	
Alumina (90%) TF Substrate		7.0	
Alumina (Ceramic Chip Carrier)	5.9	6.5	7.4
Epoxy (70% Silica) Plastic Packaging	20		23
Mulite Co-Fired		4.2	

Insulator/Substrate Material/System	CTE lower	value	upper
Conductor Material/System			
Alloy 42		4.4	
Alluminum (40% Silicon)		13.5	
Aluminum, T6061		23.6	
Boron Aluminum (20%)		12.7	
Copper, CDA 101		17.6	
Copper/Invar/Copper 20/60/20 Thick	5.7		5.8
Copper/Molybdenum/ copper 20/60/20 Thick		7	
Gold		14	
Graphite/Aluminum	4		6
Invar 36		1.6	
Invar 42		4.5	
Kovar		5	
Lead		29	
Lead (95%) Tin Solder		28	
Lead-Tin solder 60/40	23		25
Molybdenum		4.9	
Ni-clad Molybdenum	5.2		6.0
Silver	19		
Tungsten/Copper (90/10)	6.0		6.5
Tungsten		4	

Table G–2 Properties of Printed Circuit Laminates[1]

	Thermal							Mechanical
Material	Conductivity W/M-K	CTE X, Y Dir. ppm/°C	CTE Z. Dir ppm/	Max. Use Temperature °C	Glass Transition Temp. °C	Tensile Strength M Pa	Yield Strength M Pa	Elongation %
Polymer Composites:								
Polyimide Glass	0.35	12-16	40-60	215-280	250-260	345	—	
Epoxy Glass[(a)]	0.16-0.2	14-18	180	130-160	125-135	276	—	
Modified Epoxy[(b)]	-	14-16	—	—	140-150	—	—	
PTFE[(e)] Glass, Non-Woven	0.1-0.26	20	—	230-260	—	—	—	
PTFE[(e)] Glass, Woven	419-837	10-25	—	248	—	38-52	—	
Epoxy Aramid	0.12	6-8	66	—	125	68-103	—	—
Epoxy Quartz	-	6-13	62	—	125	—	—	
Polyimide Aramid	0.28	5-8	83	—	250	—	—	
Polyimide Quartz	0.35	6-12	35	—	188-250	207	—	
Epoxy - Cordierite	0.9-1.3	3.3-3.8	—	—	—	—	—	—
Modified Epoxy Aramid	—	5.5-5.6	100	—	137	—	—	
PTFE[(e)] Quartz	—	7.5-9.4	88	—	19[(d)]	—	—	
Polyimide	4.3-11.8	45-50	—	260-315	—	—	—	6-7
Metal Composites:								
Cu/Invar/Cu (20/60/20)	15-18[(c)]	5.3-5.5	16	—	N/A	310-414	170-270	36
Cu/Invar/Cu (12.5/75/12.5)	14[(c)]	4.4	—	—	N/A	380-480	240-340	
Cu/Mo/Cu	90-174	2.6	—	—	N/A	—	—	
Ni/Mo/Ni	129.8[(c)]	5.2-6	5.2-6	—	N/A	621	552	50

(a) FR-4, G-10 (b) Polyfunctional FR-4 (c) Z-direction (d) Polymorphic p (e) PTFE=Polytetrafluoroethylene

(1) See material in Technology Assessment of Laminates, IPC-TA-720; Materials for High Density Electronic Packaging and Interconnection; "Thermal Expansion Properties" chapter of Electronic Materials Handbook, Volume 1, Packaging. These values are most useful when accompanied by an indication of the ratio of reinforcement to matrix. The chemical combination of epoxy and polyimide yields bismaleimide.

Appendix H
Electrostatic Discharge

H-1.0 INTRODUCTION

H-1.1 ESD Susceptibility and Damage Prevention All electronic components containing thin conducting or insulating films are susceptible to electrostatic discharge (ESD) damage. These components include those fabricated in high speed technologies (MOS, Bipolar, GaAs), thin film technologies (resistors, integrated circuits, magnetic heads, MOS capacitors), and in future, wafer scale integration and multichip modules.

The best place for ESD protective circuitry is inside the component package.

H-1.2 Current Limiting (ESD) SM resistors/SM inductors which are unencapsulated and networks which are delaminated between pins or across the inductive or resistive element should not be counted upon to limit current during ESD events. The dielectric strength of air at sea level is ~1200 volts/mm. A 0.5 mm air gap or space can support only ~600 volts before breaking by sparking across the small air gap space between electrodes at the edge of the dielectric. SM capacitors which are un-encapsulated will also break down; some MOS capacitors are protected by preferential sparking across the small air gap space between electrodes at the edge of the dielectric. The dielectric strength of most moulding compounds is ~20,000 volts/mm.

H-1.3 Susceptible Parts and Workarounds If parts susceptible to ESD, EOS, high speed transients or latchup cannot be avoided, consult resources such as Circuits, Interconnections, and Packaging for VLSI, Decoupling and Layout of Digital Printed Circuits, or Protection of Electronic Circuits from Over-voltages. Electrical Assessment of GaAs Digital Microcircuits covers some GaAs ESD issues. High currents resulting from ESD have some predictable characteristics (1989-1991 National Institute of Science and Technology publications).

H-1.4 Assembly Process and Handling Packaging and handling of parts with ESD sensitivity must be done properly at all times, from their fabrication by the supplier through installation of the finished assemblies in the end product. In particular, they must be delivered and stored on static-free tape and reel (T/R), and shielded from outside sources of ESD. The problem is that suppliers ignorant of any danger to their product will use the cheapest packaging materials they can find. These packing materials may be ineffective at best, and sources of ESD generation on production lines at worst. Electrostatic Discharge Control, Handbook of ESD Control: The Comprehensive and Sensible Approach, ESD Program Management, and ESD from A to Z are some books addressing the assembly, handling, and transportation aspects of ESD control in the processes. Some convective reflow ovens are said to result in ESD levels of 200V on the PWA in the hot, dry, fast moving air environment. Some de-reeling environment (tape and reel material, dry air, rapid de-reeling) are said to result in ESD levels in excess of 10 kV.

H-2.0 ESD DESIGN AND CHECKLIST

H-2.1 Hardware Design In this appendix is an abbreviated design checklist addressing hardware ESD issues.

H-2.2 Assembly Process and Handling Electrostatic Discharge types:

Air Discharge is tricky; at 20 kV, arc may jump to shield but at 2 kV, arc may jump to connector pin. You cannot "accelerate" ESD air discharges by increasing voltage. You cannot simply verify ESD susceptibility of the assembly at the high end and assume that the low end is taken care of.

Rule of thumb	Concern for
20kV jumps 20 mm in air	(conductive injection)
2 kV jumps 2 mm in air	(secondary arc injection)

Contact discharge is more repeatable but less frequent in real life—except for cables with low electrostatic voltage.

H-2.2.1 Firmware/Software ESD Design Guidelines (Possibly least expensive to implement)

Refresh, at regular intervals, the following
- Interrupts
- Stop bit level for serial data output
- Latch and port output status
- Control and Selection Inputs

Check and Restore
- Program flow checkpoints
- Hardware timer for fail-safe watchdog or system reset
- Redundant data storage and comparison
- Value/Range of data in index registers
- Value/Range of data in inputs
- Frame error check
- Parity
- Checksum
- Echoing
- Periodic check for ESD induced "sleep" state
- Verify critical inputs such as interrupts and resets
- Debounce software

Graceful recovery from any ESD induced glitch
Disable interrupts during critical periods such as backup
Token establishment entering subroutine; check token on leaving SR

Memory/Registers
No-Op codes in unused memory locations
Error Traps
Unused interrupt locations trapped to error routine
Characterize CMOS for "latchup" susceptibility

H-2.2.2 Printed Board Design Guidelines

Reduce electromagnetic (EM) coupling of ESD fields with minimum loop area (Items with EMI are also used for EMI purposes)

EMI As much power and ground plane as possible, rather than conductors
EMI Power and ground grids, tied together with vias at intervals < 60 mm, rather than conductors
EMI Power and ground conductors close together, rather than spread apart
EMI No large hole (slot antenna) in power or ground plane with dimension > 50 mm, particularly near ESD ground point
EMI Vulnerable lines very close to ground or power conductor; or above ground or power grid; or above ground or power plane
EMI Unavoidable long conductors/loops treated by transposition
EMI Power and ground decoupled frequently with Multilayer Ceramic Capacitors (MLCC) [RF shunt or bypass] ~60 mm apart
EMI ESD/chassis ground plane may be simple stamped aluminum foil, 0.025 mm thick, or a laminated heat sink or very large capacitor to infinity

ESD charge injection

Keep ESD/chassis ground conductors separate from circuit ground on printed board; join ESD/chassis grounds beyond card-edge
Uninsulated portion of ESD/chassis ground on printed board with length/width aspect ratio < 5:1 and separated from circuit conductors by more than 2 mm
Uninsulated conductors/components, particularly those with sharp edges, > 20 mm from user access

H-2.2.3 Components

Reduce EM coupling with short conductors

EMI Components close together
EMI Components with densest interconnections closest together
EMI Common buss for power, ground, and signal fed from center of printed board rather than edge of printed board
I/O components as close as possible to the related I/O connector
Keep susceptible components and their conductors in those printed board areas with infrequent access; avoid printed board edges
Keep components and conductors away from "floating" metal parts, particularly those with sharp edges/burrs, e.g. screws, stampings
Tie structural metal parts to ESD/chassis ground; RFI fences and boxes may be tied to analog ground; digital bypassed busses may be tied to logic ground
Panel components, such as LEDs, switches, latches and keyboard separated from user by ESD/chassis ground or guard ring
Use differential input/output transmitter-receivers for rejection of ESD induced common mode noise
System RESET line NOT connected to long input lines
Floating inputs tied with resistor either high or low (do not use same resistor for all- See DfTestability)
Sensitive inputs filtered/protected as close to IC as possible
EMI Too much capacitance in one package adds series inductance
EMI Ferrite beads not allowed to touch each other, ground, power or signal lines.
EMI Lowest speed/ frequency/ rate of rise/fall components practical
EMI Avoid edge triggered logic
EMI ASICs with output stages tailored for rate of rise/fall
EMI Connector separated from input circuits by ESD protection networks and EMI filter(s)

H-2.2.4 Cable

EMI Use shield 0.025 mm thick and preferably of 100% coverage type and connect HF chassis ground to the shield at both ends of the cable.
If necessary, use an MLCC (1- 10 nF) as a logic ground
If necessary, add ferrite bead to signal line(s) at receiver end
EMI If possible, do not add ferrite bead to shield ground
EMI As necessary, treat extra lines in cable: clip off or remove or connect electrically in parallel.

H-2.3 CLASS 1: Sensitivity Range 0 to 1,999 Volts

Metal Oxide Semiconductor (MOS) devices, discrete, including capacitors
Integrated Circuits (IC)
Very High Speed Integrated Circuits (VHSIC)
Charge Coupled Devices (CCD)
Surface Acoustic Wave (SAW) devices
Operational Amplifiers (OP AMP)
Junction Field Effect Transistor (JFET)

Silicon Controlled Rectifier (SCR) with I_O < 0.175 A at 100°C ambient temperature
Precision Voltage Regulator Diodes: Line or Load Voltage Regulation < 0.5%
Microwave Devices (Schottky barrier diodes, point contact diodes, and other detector diodes), Frequency > 1 giga-Hertz
Thin-Film Resistors
Thick-Film Resistors where the ESD field across the film > 2 kV/mm
Hybrids utilizing Class 1 parts

H-2.4 CLASS 2: Sensitivity Range 2,000 to 3,999 Volts

Devices or Microcircuits when identified by Appendix A Test Data as Class 2

- Metal Oxide Semiconductor (MOS) devices, discrete
- Integrated Circuits (IC)
- Very High Speed Integrated Circuits (VHSIC)
- Operational Amplifiers (OP AMP)
- Junction Field Effect Transistor (JFET)

Precision Resistor Networks (Type RZ)
Hybrids utilizing Class 2 parts
Low Power Bipolar Transistors, P_T < 100 mW with IC < 100 mA

H-2.5 CLASS 3: Sensitivity Range 4,000 to 15,999 Volts

Devices or Microcircuits when identified by Appendix A Test Data as Class 3

- Metal Oxide Semiconductor (MOS) devices, discrete
- Integrated Circuits (IC)
- Very High Speed Integrated Circuits (VHSIC)
- Operational Amplifiers (OP AMP)
- Junction Field Effect Transistors (JFET)

Small Signal Diodes with power < 1 watt or IO < 1 Ampere
General Purpose Silicon Rectifier Diodes
Silicon Controlled Rectifier (SCR) with IO > 0.175 A at 100°C ambient temperature.
Low Power Bipolar Transistors with 350 mW<P/T/<100 mW and 400 mA>I/C/ >100 mA
Optoelectronic Devices (LEDs, Phototransistors, optocouplers)
Resistor Chips
Piezoelectric Crystals
Hybrids utilizing Class 3 parts

H-2.6 CLASS "4": Sensitivity Range 16,000 Volts CONSIDERED NON-ESD SENSITIVE.

The above values are considered "default" values for the part type; where vendor and part specific data exists and where the database structure permits vendor specific data, that data is to override the default value.

APPENDIX I
Solvents

I-1.0 INTRODUCTION

Surface Mount Printed Wiring Assemblies (PWA) are subjected to solvents (including water) and chemicals during manufacture, rework, repair and service. These agents include those used in soldering (alcohols, glycols and other solvents in flux vehicles at temperatures approaching 150°C), in cleaning the assembly after solder (saponifiers, neutralizers, hot water, terpene, chlorofluorocarbon (CFC) mixtures, hydrochlorofluorocarbon (HCFC) mixtures and other halogenated solvents and blends at moderate process temperatures, during removal of conformal coatings with various chemicals, and during service (hydraulic and cooling fluids and fuels in military applications; alcohols and halogenated hydrocarbons during cleanup). These solvents and chemicals can adversely affect the solder mask (SM), printed wiring board (printed board), conformal coating (CC), printed board or component legends and markings as well as degrade thin or mechanically stressed sections of plastic components. Section 7 of Electronic Materials Handbook, Volume 1, Packaging, 1989, discusses the various conformal coating (CC) chemistries. Where the adhesion of the CC, solder mask (SM) or marking to the underlying layer has been weakened (as evidenced by swelling or wrinkling), abrasion or high velocity water or high velocity solvent may lift the overlying material. Where the intimate adhesion of the CC to the SM or printed board laminate is disturbed between traces which are DC biased, electrochemical corrosion and dendriting may occur under moist environment conditions. See IPC-TR-476, IPC-SM-840, and IPC-CC-830 for discussion on dendrites, solder masks and conformal coating compatibilities. See also the section in these guidelines on various other solder mask and conformal coating issues.

Solvents under pressure, including water, can mechanically remove or chemically dissolve lubricants needed for the proper operation of switches, potentiometers and other moving components.

During servicing, alcohols and halogenated hydrocarbons may be applied to the PWA during cleanup. The PWA may be exposed to hydraulic fluids and fuels in military applications.

The D-limonene (terpene) based solvents have questionable compatibility with, or are not recommended for, short term contact at room temperatures with rubbers of nitrile, ethylene-propylene, butyl, natural, neoprene or silicone (which swells); plastics (and their alloys and blends) such as polystyrenes (PS), polycarbonates (PC), polysulfones, polyvinyl chloride (PVC), polyallomer, polyurethane (PUR), ABS, low density polyethylene (LDPE), and polyvinylidene fluoride (PVDF); nor with metals such as copper and brass. D-limonene solvent can also weaken the adhesion of printed board marking; this effect may be of significance when high velocity water and solvent washes and rinses are employed. If D-limonene is trapped under low clearance components, resulting in prolonged exposure, softening of the conformal coating or solder mask and degradation of the component plastic may occur. A general rule of thumb is that a material which survives CFC and chlorinated solvent cleaning and is water resistant should be compatible with D-limonene.

The common halogenated cleaning solvents decompose at high temperatures or in the presence of catalytic metal surfaces. Extremely high halide levels have been found in droplets of water floating on the solvent surface in the cold sump of vapor degreasing systems; in these cases, the water absorbing cartridge had failed or the solvent stabilization additives were exhausted. The halides deposit onto assemblies which are "cleaned" in the cold sump. These halogenated solvents can diffuse through the rubber seal of aluminum electrolytic capacitors; the result is the dissociation of the solvent inside the component, the release of HCl, the corrosion of the aluminum foil, and failure of the capacitor. A solution is the use of capacitors where the elastomeric seal is augmented by a hermetic, epoxy or other polymer seal effective in greatly reducing the diffusion rate of the solvent.

I-2.0 MATERIALS AFFECTED

Acrylate and epoxy solder mask materials should not be exposed for long durations to solvents and solvent systems containing methylene chloride, tetrahydrofuran, butyrolactone, N-methyl 2 pyrrolidinone, d-limonene, ethylene glycol ether, propylene oxide glycol ether, methyl alcohol, dimethylsulfoxide (DMSO) or dimethylformamide (DMF); these are constituents of systems designed to remove conformal coatings based upon acrylate and epoxy chemistries. DMF has been used as an electrolyte in aluminum electrolytic capacitors; its use has diminished because of its carcinogenic properties and its low flash point. Butyrolactone is used as an electrolyte in aluminum electrolytic capacitors, replacing DMF. The susceptibility to solvents differs between dry film SM and liquid photoimageable SM materials and between epoxy and acrylate SM materials.

Conformal coating (CC) materials differ in their response to solvents, depending upon their chemistry and curing mechanisms. Some systems are cured by heat or drying such as epoxy, acrylate, polyurethane, silicone, and fluoropolymer. Other CC materials are cured by ultraviolet (UV) light and are based upon resin systems such as epoxy,

acrylated urethane, acrylated epoxy urethane, epoxidized or acrylated silicone. Poly (para-xylylene) or Parylene™ is a unique in-situ polymerized material.

During CC removal prior to PWA rework, extreme attention must be paid to confining the solvent attack to the conformal coating; the interface between the SM and CC can be preferentially attacked. SM-CC interfacial voids may result in interconductor dendrites under DC bias and moist environment service conditions. The volume under low clearance components must be cleared of these solvents to minimize attack of the SM; vigorous DI water washing and thorough drying is required, particularly where acidic or basic "activators" are present in the solvent blend.

Activator residues may result in PWA failures due to corrosion and dendrites. Residual solvents which are relatively inert at room temperature may be detrimental at the high temperatures of solder reflow.

Silicones are susceptible to chlorinated hydrocarbons, alkanes and aromatics. Silicone gels are susceptible to swelling by CFCs and HCFCs.

Fluoropolymer CC materials such as fluoro (acrylate) and fluorinated terpolymers are susceptible to CFCs, HCFCs, ketones, halogenated hydrocarbons, esters and aromatics.

Polycarbonates are susceptible to chlorinated hydrocarbons, ketones, and bases. Diallyl phthalate (DAP) may be susceptible, at soldering temperatures, to formic or citric acids found in some flux systems.

Some phenolics, particularly those with organic filler, are susceptible to bases and ketones.

I-3.0 COMMON CLEANING SOLVENT FAMILIES

Ketones include acetone, methyl ethyl ketone, and methyl isobutyl ketone.

Aromatics include benzene, toluene, gasoline, N-methyl 2-pyrollidinone, terpene (d-limonene), and some aircraft fluids such as hydraulic or fuel. Halogenated hydrocarbons include CFC and CFC blends with methylene chloride, methanol, ethanol; hydrochlorofluorocarbon (HCFC); hydrofluorocarbon (HFC); and chlorinated hydrocarbons (methylene chloride, trichloroethane, trichloroethylene, and methyl chloroform).

Bases include ammonia, amines, neutralizers and saponifiers.

Alcohols (organic bases) include methyl, ethyl, propyl, and butyl alcohols.

Esters (organic salts) include butyl acetate and ethyl acetate.

I-4.0 HCFC BLEND AND OTHER DATA

Plastic Solvent Compatibility (Boiling liquid, 5 minutes)

HCFC Blend HCFC 141b/HCFC 123/ 2.5% Methyl Alcohol/ 0.3% Stabilizer
Incompatible: Acrylonitrile Butadiene Styrene (ABS), Acrylics, Cellulosics, Polycarbonate (PC), Polystyrene, Butyl Rubber Adhesive
Probably incompatible: Polyphenylene Oxide (PPO)

CFC-113 + Methyl Alcohol
Incompatible: Cellulosics
Probably incompatible: Polystyrene

Data primarily for the equipment designer, Long Duration Exposure

Plastic-Solvent Compatibility (Liquid at 50°C, 24 hours) might be specified but no extrapolation is possible to conditions such as 100°C or Boiling Point, 1 minute (cleaning) or 25°C, 24 hours (trapped between a component and printed board).

Dupont Hydrocarbon Solvent (Axarel)
Incompatible: Cellulosics, Polyacrylate, Polycarbonate (PC), Polystyrene
Probably incompatible: Acrylonitrile Butadiene Styrene (ABS), Acrylics, Ionomer, Polyphenylene Oxide (PPO), Polypropylene, Polyvinyl Chloride (PVC), Chlorinated Polyvinyl Chloride (CPVC).
Solder mask or conformal coating may be affected if the solvent is trapped under low clearance components.

Elastomer-Solvent Compatibility (Extractables, boiling, 8 hours)

HCFC Blend HCFC 141b/HCFC 123/ 2.5% Methyl Alcohol/ 0.3% Stabilizer
< 1%: Fluoroelastomer (Viton B), Perfluoroelastomer (Kalrez)
< 5%: Polyurethane, Chlorosulfonated Polyethylene, Polyester TPE, Polysiloxane (Silicones), Polysulfide FA/ST, Fluoroelastomer (Viton A)
< 10%: Isobutylene-isoprene, Natural Polyisoprene
> 10%: Acrylonitrile Butadiene, Styrene-Butadiene, Polychloroprene, Ethylene/Propylene Terpolymer

CFC-113 + Methyl Alcohol
< 5%: Polyurethane, Isobutylene-isoprene, Polyester TPE, Natural Polyisoprene, Polysiloxane (Silicones), Polysulfide, Fluoroelastomer (Viton A)
< 10%: Styrene-Butadiene, Polychloroprene,
> 10%: Acrylonitrile Butadiene, Ethylene/ Propylene Terpolymer

Elastomer Solvent Compatibility (% Weight Change, Liquid, 50°C, 168 hours) (For most of these materials, % Linear Swell is approximately ⅓ the % Weight Change).

Dupont Hydrocarbon Solvent (Axarel)

< 5%: Thiokol FA, Fluoroelastomer (Viton VT-R-6186), Perfluoroelastomer (Kalrez)

< 50%: Styrene- Butadiene Rubber (SBR), Ethylene-Propylene- Diene Monomer (EPDM), (Nordel), Chlorosulfonated Polyethylene, Polychloroprene, Polyester Thermoplastic Elastomer (TPE), Elastomer Alloy Thermoplastic Vulcanizable (TPV) (Alcryn), Thiokol ST, Fluoroelastomer (Viton- A/ -B/ -GF)

> 50%: Butyl Rubber, Natural Rubber, Acrylonitrile-Butadiene Rubber (NBR), Silicone, Ethylene-Acrylic Co-Polymer (Vamac)

Appendix J
Design for Testability

J-1.0 DESIGN FOR TESTABILITY (DfT)

DfT is the process intended to incorporate the following three goals:

J-1.1 Controllability The ability to establish a specific signal value at each node in a circuit by setting values on the circuit's inputs is termed controllability. Barriers include decoders, circuits with local or global feedback, oscillators, clock generators, and counters with no parallel preset/reset/clear inputs. Solutions include increased test or control points at primary inputs.

Solutions for ASICs include built-in self-test stimulus generator/response detector-analyzer circuits to check RAM and ROM functions as well as scan circuits to check combinational functions. Techniques for PWAs include additional test pads and incorporation of IEEE 1149.1 Boundary Scan ICs.

J-1.2 Observability/Visibility The ability to determine the signal value at any node in a circuit by controlling the circuit's inputs and observing its outputs. Barriers include unique input patterns or lengthy complex input patterns to propagate the state of an internal node to a circuit output, sequential circuits, circuits with global feedback, embedded RAMs, ROMs, PLAs, concurrent error-checking circuits, and circuits with redundant nodes.

Solutions include incorporation of increased test or observation points at primary outputs, incorporation of the ability to interrupt chains and feedback loops, and partitioning of the circuit into more tractable clusters. Specialized techniques for ASICs include the quiescent current test method (Iddq) techniques which add a grid of built-in test points. Techniques for SM PWAs include additional test pads and incorporation of IEEE 1149.1 Boundary Scan ICs, as well as inclusion of printed board jumpers which are opened or shorted for test purposes.

J-1.3 Partitioning Partitioning refers to reducing a complex circuit into a set of interactive subcircuits.

J-2.0 STANDARDS

J-2.1 General Other IEEE 1149.X proposed standards include:

1. P1149.2, Parallel/Serial Scan Based Testing (Chips, Board, System) Combinatorial Scan-Access Port (SAP) Controller;
2. P1149.3, Family of Buses, Direct Access between Test Resources and UUT Internal Nodes. (Testability features placeable on board or system)
3. 1149.5, Test and Maintenance Backplane Bus

J-2.2 Testability Aspects of Design for Testability for SM PWAs are discussed in the standards listed below. Note that these documents do not address ASIC level DfT issues.

1. TP-101A, Testability Guidelines
2. IPC-ET-652, Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards
3. IPC-D-275, Design Standard for Rigid Printed Boards and Rigid Printed Board Assemblies

J-3.0 SUBSTRATE TESTING

Testing is one means of helping to reduce costs and increase the reliability of SMT assemblies. Systems requiring SMT do so because of size, weight, reliability, and performing considerations. SMT assemblies can be quite complex containing thousands of networks to interconnect ICs. Performing tests through the substrate fabrication processes are necessary to achieve desired yields.

A typical SMT approach is to fully test the bare substrate interconnections prior to component mounting. The bare substrate is 100% short and open tested using a bed-of-nails fixture or moving probe system. The purpose of this test is to isolate defects prior to mounting expensive components to the substrate. By verifying the substrate interconnections before SMT assembly, final test yields are increased and potentially expensive rework is reduced. Most defects can be found using this technique.

Substrate defects can be a significant issue in SMT processing because with increasing complexity and density it is more difficult to produce high yields in substrate processing. Some of the common substrate defects are open vias, conductor to conductor shorts, open conductors, layer to layer shorts, and high resistance vias or conductors. These defects are a result of the processing such as undercutting vias, particulate contaminants (i.e. on photoresist), interlayer voids, poor metal-to-polymer adhesion, contaminated plating baths, or uncontrolled conductor etching.

Emerging technologies such as imbedding chips within the substrate interconnect structure creates a problem in testing the substrate and chips separately. Thus, higher substrate yields are critical. It is also extremely important to 100% test the bare substrate although engineers may be tempted not to in order to save time and money. However, in a SMT printed board, 50% of the faults can be traced to the bare substrate. The fault probabilities are even greater with emerging technologies (Flip-chip, TAB, etc.) because of

the increase in complexity and density of the interconnects.

J-4.0 CHIP TESTING

Testing of components and bare dice are typically performed by the IC vendor who applies a variety of tests. In the case of packaged dice, they are typically burned-in, screened, and separated into categories based on speed, temperature, and performance attributes. Other component testing includes a full vector set, full parametrics, at clock speed rates, and temperature testing. Bare chips do not or cannot have these tests performed. These tests are often done at the wafer level, however, before the wafer is separated into individual die. Bare chip testing is the testing of semiconductor devices in bare chip form after they have been diced from the wafer. In this form, it is difficult and costly to fixture the individually cut die for test purposes. Most suppliers, therefore, perform limited testing of chips on the wafer and no testing after dicing from the wafer. Thus, the main obstacle in using future technologies is obtaining quality ICs in unpackaged formats. The availability and confidence levels of these ICs are issues requiring industry wide resolution so these technologies can be implemented cost effectively.

J-5.0 PROBLEMS AND ISSUES OF UNPACKAGED ICs

J-5.1 Availability Obtaining known "good" unpackaged ICs, which are referred to as known good die, or KGD is difficult. More industry infrastructure development and standardization are needed to improve the situation. Improvements are being made since the IC vendors have recognized the market for unpackaged ICs such as TAB, flip-chip, and so on.

J-5.2 Confidence Level Whether the die is packaged or unpackaged it is imperative that the ICs have a high known confidence level. The goal is to yield fully functional ICs after assembly processes, over the design temperature range and operating speeds, after assembly burn-in or environmental stress screening (ESS), and after a given time in the field.

J-5.3 Vendor Concerns IC vendors are reluctant to supply bare unpackaged dice or chips for a variety of reasons. They include a loss of revenue from value added processes such as packaging and testing. Testing of bare chips is difficult and expensive, requiring specialized tooling and techniques. Interruptions to standard procedures and process flows require high volumes to justify the expense and risk of selling bare dice.

J-5.4 User Concerns Under existing conditions, the best way of ensuring bare chip availability and quality is for a company to produce and test its own supply. However, most companies desiring to use the emerging technologies are not vertically integrated. Thus, most users must rely on IC vendors to provide quality components for their assembly needs. Therefore, the user must be aware that the unpackaged dice will not be procured with the same performance or reliability guarantees as packaged ICs.

J-5.5 Standards Industry standards for SMT design and assembly is currently well defined. Future technologies requiring bare chips, however, is in its infancy. The basic problems include the lack of detailed information on the mechanical, electrical and material properties of the bare chip and the lack of industry standards for such issues as chip sizes and shapes. Some of these issues are being addressed but resolution will not be in the near future.

J-6.0 ASSEMBLY TESTING

Multilayer SMT printed board designs bury many signals on internal layers and bring them to the top layer with a via at the point of bonding as a means of providing test system access. Monitoring of these signals with a tester is possible by creating special pads for test probes. Accessibility of these signals is performed by identifying which nodes will be checked or accessed during the test and determining the appropriate set of vectors to exercise them. Automatically routing internal signals to test pads on an external layer allows critical nodes to be probe tested.

The goal of assembly level testing is to verify that the components were successfully connected to the substrate and that the component I/Os are functioning. At this testing level, it is assumed that both the substrate and individual components were previously tested fully. This test does not test the assembly at full clock speeds and does not test each IC on the board at the gate level.

Emerging technologies, such as multichip modules (MCM), require the features of both component level and assembly level testing. In some cases, testing at full clock and data rates may also be required. Testing down to the gate level is difficult since a MCM assembly can have over 1 million gates. Simulation modelling is one solution but until an industry standard is adopted most modelling of functionality and performance will be ad hoc.

J-7.0 APPROACHES TO SMT TESTING

Automated testers which work by applying a series of input patterns (test vectors) to the device-under-test (DUT) and looking for a predefined sequence of outputs are in use for many applications. But as signal density and board complexity increases, it becomes too time consuming to apply all possible input patterns to each DUT. Doing so would vastly increase the time each board spends on the test fixture. The key to streamlining the testing process is choosing that minimum group of test vectors which ensures full or maximum coverage of possible faults in a design.

There are also issues associated with the type of test equipment used. Each tester has capabilities and limits which can affect its ability to check product functionality. These should be catalogued on-line and automatically enforced so that all test programs developed will work properly with the target test equipment. There are several software products available which streamline test vector generation and simplified simulation can be useful. The major methods of improving testability follow in the sections below.

J-7.1 Ad Hoc Techniques Test access pins, multiplexers, control gates, test buses, embedded test software and other cases where specific approaches are used to improve the controllability, observability, and partitioning.

J-7.2 Structured Techniques Scan methods such as level sensitive scan design (LSSD), scan set, and random access scan alter sequential storage elements within the device logic to act as serial shift registers. These scan techniques allow automatic test generation and can be combined with boundary-scan and built-in-self-test (BIST) approaches for a very comprehensive approach to test.

J-7.2.1 Boundary-Scan Boundary scan is a structure digital DFT technique which places a serial access path (scan path) around the periphery (boundary) of the device logic. Its main purpose is to provide test access for verifying the integrity of interconnects at the assembly level by means of a 4-wire serial bus. The boundary-scan architecture allows three main types of testing.

1. External Test: This mode allows verifying the interconnections between the IC and external test equipment or other ICs, including the circuit traces, bond wires backplanes, and connectors. Open circuit, bridging fault or stack fault conditions can also be detected.
2. Internal Test: Internal test allows individual components to be tested as though they were free-standing devices. The large serial vectors required and lengthy run time are drawbacks to this method. A more effective means of internal test is boundary-scan coupled with at speed BIST circuitry.
3. Sample Mode: This feature allows monitoring of device I/O pins during normal operation of the system without affecting circuit operation.

Although boundary-scan is primarily aimed at dc type testing the basic IEEE 1149.1/JTAG architecture can be extended to achieve other test methods.

J-7.2.2 BIST BIST is synonymous with built-in-test (BIT) and self-test. It can be defined as the capability of a system to test itself with little or no external test equipment, or manual intervention techniques are used to create on-chip hardware for input stimulus generation and output response evaluation. Functional and structural techniques that allow circuit modified registers can be used to provide stimulus and response capability.

J-7.2.3 Boundary-Scan Coupled with BIST Boundary-scan coupled with BIST provides a hierarchical approach to testing from the wafer level to system level. Test routines developed by the IC manufacturers can be reused at all successive higher levels of assembly.

J-7.3 Resistive Testing with Flying Probes The most straight forward method of testing is with two moving probes using resistance to detect faults. This method eliminates dependence on expensive fixtures and provides a simple, straightforward way of testing. Probe tip designs, mechanical stage accuracy, and pad damage issues must be dealt with.

J-7.4 Capacitance Testing Capacitance testing is done with a single moving probe. New capacitance measurements are made with reference to an external conductive reference plate or an internal substrate conductive plane. The speed advantage over resistance testing is obvious since the number of tests required is equal to the total number of net nodes on the substrate, a linear function of complexity.

J-7.5 Combined Resistance/Capacitance Testing To eliminate lengthy resistance test time and improve the quality of the test method, combining both capacitance and resistance testing can be used. When capacitance and resistance instrumentation are combined for testing, it only takes a software change to perform other tests and diagnostics.

J-7.6 Glow Discharge Glow discharge testing provides a way of optically detecting opens and shorts. The substrate under test is placed in a chamber which is evaluated and then back-filled with an inert gas such as argon. A single moving probe contacts one node of each network to apply a voltage to the net which then appears on all top surface nodes of the net. The visible glow of each node is viewed through a window in the top of the changer by a scanning photometer.

J-7.7 Automatic Optical Inspection (AOI) AOI can detect feature defects that might cause electrical opens and shorts. AOI is computational intensive and generally utilizes highly specialized image analysis data processors to achieve acceptable inspection time. A major issue involves achieving adequate image contrast to reduce the inspection problem to a binary (black/white) image. AOI and non-contact probing are desirable in situations where hard probing can cause damage which reduces process yields. AOI

can also be used as a process control measure once the process is under control.

J-8.0 ISSUES AND CONCERNS OF TESTING

J-8.1 Test Equipment The tester used with certain high-density assembly technologies may itself have limitations which must be considered. As single line conductor pitch continues to fall, it becomes increasingly difficult to probe all points, even if they are located on an outer layer. Probe points on the test head become increasingly fragile. Coplanarity of the test head and assembly is also a concern.

J-8.2 Test Points The distribution of test points routed on or brought to an outside layer is also an issue. If they are clustered together, too much pressure may be brought to bear on a small area of fragile substrate. In particular, dense circuits may have difficulty placing test points for all desired nodes on an outside layer.

J-8.3 Costs Cost issues also need to be considered. Reducing the test probe grid below 1.25 mm results in more expensive test fixtures. Test probes with these spacings are quite fragile and may require frequent placement. Clam shell fixtures, which can simultaneously probe both sides of an assembly, if required, are also costly. In addition, clam shell fixtures may be subject to timing problems since back side wires in the test fixtures may be longer than front side ones.

J-8.4 CAD/CAE Software A host of issues are associated with the hardware and software platform on which CAD/CAE software runs. They are beyond the scope of this document. However, suffice it to say that CAD/CAE software vendors must be attentive to the changing trends in technologies; even with a large installed base, proprietary platforms are already proving to be obsolete.

Appendix K
Design for Manufacturability and Assembly Checklist

K-1.0 SUMMARY

Definition of manufacturability: a measure of the ease or simplicity with which a product can be manufactured or assembled.

These guidelines deal with Design for Manufacturability (DfM) primarily at the detailed component and process levels and the focus is on doing things right, particularly with respect to improving quality and reliability; if the DfM process is used early in the design process, the focus can be on doing the right things in terms of system organization and setting testability expectations. More benefits are derived from early use of conceptual design and DfM processes.

Section Topics:

- Minimize number of parts
- Minimize number of part numbers
- Design for robustness (Design of Experiments)
- Eliminate adjustments
- Design for efficient and adequate inspection and testing (testability)
- Eliminate engineering changes on released products
- Make assembly easy and foolproof (Poka-Yoke)
- Use repeatable, well-understood processes
- Choose parts that can survive (are compatible with) process operations including rework, repair and maintenance
- Choose or design process for compatibility with susceptible parts
- Layout parts for reliable process completion

Table K-1 Checklist for Design for Manufacturability and Assembly

GUIDELINE	AREA OF QUALITY/RELIABILITY IMPROVEMENT
Minimize Number of Parts	
Fewer part and assembly drawings Less complicated assemblies Fewer parts to hold to required quality characteristics Fewer parts to drift or fail Fewer solder attachments to make or fail 'Design Guidelines for Quality Improvement'	Fewer documents to control Lower assembly error rate Higher consistency of part quality Higher reliability
Minimize Number of Parts	
Fewer variations of like parts	Lower assembly error rate
Design for Robustness (Design of Experiments)	
Low sensitivity to component variability PTH, via aspect ratio (AR) < 5:1 temperature or use blind/buried vias Use standard or preferred parts (EIA/JEDEC registered) Use compatible SM land patterns (IPC-SM-782)	Higher first-pass yield and less degradation of performance over time Less sensitivity to cycling and thermal shock, lower failure rate Fewer new failure modes and mechanisms Fewer suppliers to manage Widen process window Increase assembly yield
Eliminate Adjustments	
No assembly adjustment errors Eliminate adjustable components with high failure rates Eliminate change in adjustments under vibration and shock Provide adjustments and compensation through software Consider digitally switched resistor network	Higher first-pass yield Lower failure rate
Design for Efficient and Adequate Inspection and Testing (Testability)	
Less mistaking "good" for "bad" product and vice versa Less effort to locate defects Better control over rework/repair	Truer assessment of quality, less unnecessary rework Faster diagnosis to root cause Less service/maintenance time More "up" time Less part damage

GUIDELINE	AREA OF QUALITY/RELIABILITY IMPROVEMENT
Eliminate Engineering Changes on Released Products	
Fewer errors due to changeovers & multiple revisions/versions	Lower assembly error rate
Make Assembly Easy and Foolproof (Poka-Yoke)	
No "force fitting" of parts Parts cannot be assembled wrong Obvious when parts are missing or wrong orientation Assembly tooling designed into part (self-aligning/securing)	Less damage to parts, faster and better serviceability Lower assembly error rate
Use Repeatable, Well-Understood Processes	
Part quality easy to control Assembly quality easy to control	Higher part yield Higher assembly yield
Choose Parts that Can Survive (are Compatible with) Process Operations including Rework, Repair and Maintenance	
Less damage to parts Less part degradation or latent damage through prior evaluation Plastic Encapsulated Surface Mount Components - IPC-SM-786 SM Connectors - IPC-C-408 Other SM Components - IPC's "Solvent Compatibility" No silver termination finish No nickel termination finish No thick gold printed board or termination Minimize number of TH components Maximize printed board Tg (glass transition temperature) Printed board thickness compatible with placement machine Dry film solder mask and solder paste compatibility Components and solder mask result in adequate clearance to printed board	Higher yield Higher reliability Avoid silver leaching, weak solder joint Increase solderability, joint strength Increase solder joint visual yield finish Lower defects due to solder bridging wider TH and SM process latitude Decrease hand loading, manual soldering Decrease patent and latent printed board damage at high process temperatures Minimize solder balls Enhanced cleaning. Higher SIR PWA robust to dendrite formation
Choose or Design Process for Compatibility with Susceptible Parts	
Less part damage or degradation Ceramic components thermal shock < 4°C/second Sensitive components preheated so that $\Delta T < 100°C$ Susceptible Plastic Encapsulated Surface Mount Components handled per IPC-SM-786 Don't impact ceramic parts with pick and place tooling Reflow process adjusted for thermal unbalance due to thermal masses of parts (PGA, Heat Sinks) Dry susceptible substrates before reflow Component terminations not used for in-circuit testing	Higher yield Higher reliability
Layout Parts for Reliable Process Completion	
Less damage to parts during handling and assembly Orient parts for non-interfering single axis insertion Sequence parts for insertion for easy disassembly Orient similar parts similarly Parts not hanging over solder quality (own or neighboring parts). No shadowing Parts can automatically be placed or inserted	Higher yield, higher reliability Less part damage Easier rework, repair and maintenance Fewer orientation sensitive bridging or solder joint failure modes Consistent solder joint Lower assembly error rate

Appendix L
Corrosion Basics and Checklist

L-1.0 CORROSION BASICS

The result of corrosion is material loss due to corrosion of the metallic conductors, permanent or intermittent continuity loss due to build up of non-conductive corrosion residues (particularly between contacts) and permanent or intermittent shorts due to build up of conductive corrosion residues and conductive metal dendrites. Corrosion accelerates the failure of components under cyclic fatigue conditions. Corrosion can also disrupt painted or plated product coatings. Surfaces roughened by corrosion are less effective as sealing surfaces. Water increases the oxidation rate of oxidants such as SO_2, SO_3 and O_2. Water greatly increases the corrosion rate and metal migration growth rate of halides such as chloride and fluoride. Water enhances galvanic corrosion in the presence of dissimilar metallic finishes; this issue is critical for EMI gaskets, EMI seals and brazed joints to electroplated structures in ceramic packages. In the presence of nutrient materials, water increases fungus growth; the fungi release organic acids in their waste products.

The oxides of tin, nickel and copper are not good conductors. Low interfacial pressure contacts to these metals can become resistive or intermittent.

Salt atmosphere/spray and flowing corrosive gas atmosphere are excellent sources of hydrolyzable, conductive contamination + water + oxygen. Salt atmosphere/spray stress is required in military systems but is not commonly encountered in commercial situations; it normally results in the detection of plating porosity, but is also known to result in loss of hermeticity in sealed packages as well as loss of legibility of component marking.

Office and factory dusts have been found to contain high levels of chlorides; water pastes made with dust from the tops of benches and fume hoods are highly conductive. The atmosphere of paper mills contains acidic sulfide and sulfate compounds. Unfiltered forced cooling air can contribute to premature failure of peripherals and system.

The common halogenated cleaning solvents decompose at high temperatures or in the presence of catalytic metal surfaces. Extremely high halide levels have been found in droplets of water floating on the solvent surface in the cold sump of vapor degreasing systems; in these cases, the water absorbing cartridge had failed or the solvent stabilization additives were exhausted. The halides deposit onto assemblies which are "cleaned" in the cold sump.

A typical source of hydrolyzable or ionizable contaminants which result in corrosion in electronics is human fingerprints, spittle, and food. Fingerprints also contribute oily or greasy residues which keep the conformal coatings from fully protecting the conductors and lands from electrochemical corrosion.

L-2.0 CORROSION OF THE PWA

The common insulation system in a PWA is the printed board, its solder mask and any conformal coating. Adsorption of water or condensation of water vapor on the surface of insulators with dissolution of hydrolyzable contaminants results in the subsequent loss of Surface Insulation Resistance (SIR); this effect is seen particularly on porous surfaces such as uncoated printed boards which have been contaminated with hydrolyzable materials and have not been scrupulously cleaned and can lead to electrochemical corrosion effects such as metal migration and dendrites. Metallic dendrites of the common electronic metals (silver, copper, tin, lead, gold) have been found on the surface of PWAs contaminated with chlorides and operated under high humidity.

Dendrites have also been found within the bulk of the printed board where voids allowed entrapment of conductive solutions and within delaminated areas of IC's where flux residues were found. See "A Review of Corrosion Failure Mechanisms during Accelerated Tests." The presence of water, DC bias and ionizable contaminants at the interface between the resin matrix and glass fibers between PTHs, vias and conductors lead to interfacial electrochemical corrosion and dendrites or Conductive Anodic Filaments (CAF). See Appendix C. See also IPC-TR-476.

L-3.0 CORROSION IN COMPONENTS

Common halogenated solvents can and have diffused through the rubber seal of aluminum electrolytic capacitors; the result is the dissociation of the solvent inside the component, the release of HCl, the corrosion of the aluminum foil, and failure of the capacitor. A solution is the use of capacitors where the elastomeric seal is augmented by a hermetic or epoxy seal.

Absorption in the bulk of insulators with dissolution of hydrolyzable contaminants results in the subsequent loss of bulk Moisture Insulation Resistance (MIR) particularly in printed boards, dielectric film capacitors and plastic encapsulated electronic components such as integrated circuits, networks, and hybrids. Dendrites have also been found within delaminated areas of IC's where flux residues were found.

L-4.0 OTHER EFFECTS OF WATER AND WATER VAPOR

Absorption of water in the bulk of the insulating film of capacitors results in increased dissipation factor and increased leakage current. Absorption of water by specific

plastic and gasket materials (up to 1% water by weight) results in swelling; cyclic changes in humidity can result in "creeping" of the plastic or gasket material. Very low levels of water vapor (low Relative Humidity or RH) allow ElectroStatic Discharge (ESD) voltages to build up. Chemisorption of water into polymer systems such as molding compounds results in a lower T_g, lower strength and increased total thermal expansion.

L-5.0 FRETTING "CORROSION"

This category of corrosion is a mishmash of failure of contacts from two causes:

- In contrast to the good performance of gold-gold (gold to gold) contacts at low contact pressures and low circuit energy levels or of tin-tin contacts at high contact pressures and high circuit energy levels, gold-tin contacts fail even at high pressures and high energy levels due to the formation of gold/tin intermetallics with low conductivity at the contact points due to small relative motions between the contacts (micromotion). Separable connectors and sockets for components such as ICs have contributed to system failure when the gold/tin intermetallics are formed. The micromotions can be caused by power cycling of the component as well as shock, vibration or temperature cycling of the system.
- In the presence of hydrocarbon vapors and relative contact movement as in relays, platinum group metal contacts catalyze the development of an insulating polymeric film; the source of the vapors can be the housing of a relay. In the presence of silicone vapors, electrical arcing and relative contact movement, metal contacts develop an insulating silica film.

L-6.0 CORROSION DESIGN CHECKLIST

- Identify process, service, rework and repair environments and chemicals, particularly:
  - Rapid transitions between high temperature/high humidity and low temperature with immediate or continuing operation.
  - Long term low or battery power operation at high relative humidity.
- Mitigate effects of long term low power operation by requiring that low power ICs and other components with DC bias be free of delamination and cracking between encapsulant and the surface of the IC or substrate; risk sites are covered with void free laminate, solder mask or conformal coating (CC). The CC should demonstrate no delamination, mealing or vesication after exposure to high humidity/DC bias (e.g. by absence of delamination with Scanning Acoustic Microscopy).
- Assure that substrate conductor and component lead spacings are suitable for the environmental conditions of the product (humidity, contaminating dust, thermal cycling, bias, corrosive gases) where no additional conformal coating is required. Minimum spacings from conductors to (conductor, mounting hole, component terminals) and from barrels to inner plane conductors and other barrels are used only where needed. Also a DfM guideline.
- Identify and design against potential damage to insulating or moisture barrier solder mask or conformal coating by stresses such as high temperature, UV, and ozone exposure; for partially cured coatings, very low temperature can cause cracking.
- In environments with anticipated vibration or thermomechanical movements due to temperature cycling, separable connectors and contacts are immobilized. Particularly applies to the active catalyst platinum family, including gold, to prevent the formation of insulating polymers from condensible carbonaceous vapors. See also "fretting corrosion" below.
- Identify susceptible metals used in the components and general design; for those metals, quantify performance under anticipated corrosion stress.
- Design assemblies and choose components which are easy to keep clean or are easy to clean. Minimum use of EIAJ "O" clearance components, particularly where using water soluble flux. Minimum use of discrete component spacers which introduce multiple crevices (sugar or adhesive spot under components is OK). Also a DfM guideline.
- The assembly process requires maintenance of clean condition of components and assemblies (e.g. by the use of gloves during handling); clean ambient conditions during laminate handling, lamination, storage; cleaning of printed board prior to solder mask application. There is no hydrophilic solvent (e.g. polyglycol) in fluxes or soldering oil. Solvent or water mechanically removed prior to air dry (e.g. air knives); nonpolar solvent used to remove organics which trap or mask water soluble contaminants; polar solvents or hot DI water used to remove ionizable contaminants; ultrasonic cleaning or high solvent velocity to get between crevices. Where applicable, periodic SIR testing is conducted to verify continued efficacy of the cleaning method.
- Avoid all identified potential moisture traps associated with components, including open cavity packages sealed with polymers and low clearance packages over bare conductors. Corrodible portions inside the cavity are sealed with hydrophobic materials such as silicone. Conductors are sealed with solder mask or conformal coating prior to assembly or component clearance increased to effect complete cleaning.
- Avoid all identified, exposed galvanic couples such as

terminations of copper/nickel/gold which are sheared after plating (e.g. exposed base metals on the edges of contacts). These conditions can also lead to tarnish creep, the extension of corrosion products of copper over the gold. See a sample galvanic compatibility table below.

- Identify mechanical stress levels in susceptible metal parts (particularly formed terminations for possible contribution to stress corrosion or plating discontinuities); alternatively, metal parts are formed in the annealed state and postplated.
- Identify susceptible ceramic package brazed and plated terminations which may have brazed joints of metals constituting galvanic couples, may have exposed plated interfaces, and may have been or need to be trimmed and/or formed after plating.
- Use components which do not release corrosive materials. Wet slug tantalum with sulfuric acid electrolyte is not recommended for new designs. Avoid aluminum electrolytics with dimethyl formamide electrolyte which degrades solder mask and conformal coatings. Orient vent plugs of unavoidable electrolytic capacitors to minimize damage consequent to component failure—face vent plugs away from substrate.
- Identify and if possible avoid galvanic corrosion couples; these practices may mitigate consequences:
  - Plating is to be complete with no exposed interfaces in plating systems such as copper overplated with solder, tin, or gold. Alternatively, interpose nickel plating between the copper and the overplate.
  - Interpose an intermediate compatible material. For instance, for a steel screw fastened to aluminum, interpose a washer plated with cadmium (an environmental no-no) or use "active" stainless steel for the screw where the S/S passivation tends to isolate the screw.
  - Selectively metallic plate as required for reliable electrical contact between pressure contacts; e.g. gold to gold or tin to tin but not gold to tin (to avoid "fretting" corrosion).
  - Coat surfaces (with polymeric or conversion material) for insulation and moisture exclusion.
  - Anodically finish for insulation and moisture exclusion but be very careful; the coating is thin and brittle and entrapped residual anodic processing fluids are corrosive.
  - Design so that cathodic metal area is much smaller than the anodic metal area.
- Assure that fretting "corrosion" has been minimized or eliminated:
  - The need for contact lubricants has been investigated and satisfied.
  - Contact finish and thickness/porosity/smoothness is appropriate to the use environment, including frequency of reconnections and current/voltage conditions.
  - Contacts are gold to gold or tin to tin but not gold to tin.
  - Card mounting stresses and flex circuit flexures (static or dynamic vibration) are controlled by clamps, screws, hold-downs; the stresses are not transmitted to the connector or to the contacts.
- Identify conditions at possible electrochemical corrosion risk sites:
  - bare metal
  - tight spacing (very small diameter vias, complex mechanical fitted parts, connectors, switches, variable elements...)
  - relative humidity 65% or condensed water films and droplets
  - ionizable contamination
  - conductors with DC potential (particularly between leads of fine pitch elements and where pin assignment is optional, avoid large potential differences between adjacent pins of connectors);
- Pressure contacts are sealed from condensing moisture, high humidity, and corrosive gases; conformal rubber seals under continuous high pressure appears to be effective. Be cautious of compression set effect of rubbers at low temperatures.
- Avoid exposed silver plating, silver pastes, and silver adhesives; overplate silver conductor material with nickel or conformally coat or locate the component so that water will not condense and run onto the silver. Includes MLCC, DIP, rotary and slide switch, variable resistor and buzzer packages.
- Tent all vias and PTHs on both ends if using active water soluble flux (paste or liquid); alternatively, open vias and PTHs do not terminate under a component with tight clearance. A third alternative is to fill the vias and PTHs with solder, epoxy or modified solder mask/conformal coating material. These techniques minimize barrel corrosion due to flux entrapment and avoid test fixture corrosion and loss of SIR due to drips of liquid flux.
- Hydrolyzable materials completely removed from the PWA prior to application of any solder mask; similar cleaning prior to any conformal coating application. This is critical where water soluble flux systems are used; otherwise, mealing and vesication can result under high RH conditions.
- Avoid conductive anodic filament growth (CAF). Evaluate printed board suppliers for delamination of solder mask between conductors and laminate voids

between conductors or barrels pre- and post-assembly process stresses. To break possible CAF paths, use a minimum of 2 plies for all layers and smooth and seal board edges.

- printed board supplier's inspection area is controlled for humidity, temperature, cleanliness. Volume resistance is a strong function of temperature changes, surface resistance (SIR) is a strong function of humidity and humidity changes, and delamination/measling/vesication are functions of laminate cleaning and cleanliness.

L-6.1 Galvanic Corrosion See also Sections 4 and 9, ASM Electronic Materials Handbook, Volume 1, Packaging, 1989; Contamination Effects on Electronic Products by Carl Tautscher, Marcel Dekker, Inc., 1991, ISBN 0-8247-8423-5. For sources of Ecorr vs. SCE, see Galvanic and Pitting Corrosion-Field and Lab Studies, ASTM STP 576, 1976

Caution

Aluminum - 1% Silicon - 0.5% Copper alloy used for integrated circuit metallization contains Al_2Cu (Q phase) which has a large oxidation (galvanic) potential with respect to aluminum; in the presence of moisture, rapid oxidation of aluminum occurs in the vicinity of copper precipitates - and pits grow in the aluminum.

Table L–1 Galvanic Compatibility of Metals

METAL	GROUP I	GROUP II	GROUP III	GROUP IV
ANODIC - Corroded				
Magnesium/Magnesium Alloys	X			
Zinc/Zinc Plating	X	X		
Aluminum filled (silver plated) Elastomer die Cut Edge (-740)				
Aluminum/Aluminum alloys (-740 to -840 mV)	X	X		
Beryllium	X	X		
Chromium Plating	X	X		
Tungsten	X	X		
Molybdenum	X	X		
Cadmium Plating (Restricted)		X	X	
Carbon Steel, Cast Iron		X	X	
Stainless Steel, Active		X	X	
Lead, Tin-Lead Solder		X	X	
Tin/Tin Plating (-440 V)		X	X	
Tin/Indium		X	X	
Nickel/Nickel Plating, Active (-250 mV)		X	X	
Leaded Brass/Bronze		X	X	
Copper-Zinc Alloys (Brasses)				
Naval Brass		X	X	
Brass, Commercial Yellow			X	X
Copper/Copper Alloys (-244 mV)			X	X
Beryllium Copper			X	X
Copper-Tin Alloys (Bronzes)				
Copper-Nickel Alloys			X	X
Aluminum or copper filled (silver plated) Elastomer (-190 to -200 mV)				
Monel (-125 mV)			X	X
Silver Solder			X	X
Nickel, Nickel Plating, Passive			X	X
Cobalt, Cobalt/Nickel alloy			X	X
Stainless Steel, Passive			X	X
Silver-filled Elastomers (-50 mV)				X
Silver/Silver alloys (-25 mV)				X
Silver-filled Films				X
Graphite/Carbon				X
Rhodium				X
Palladium				X
Titanium				X
Gold, Platinum, Gold/Platinum Alloys				X
CATHODIC - Protected				X

Appendix M
Solder Joint Variability

M-1.0 SOLDER JOINT VARIABILITY

Appendix A describes the design parameters which determine the mean cycles to failure. The Weibull parameter describes the variability in the response of the solder attachment and the individual solder joints due to manufacturing or processing conditions as well as the inherent variability in wear-out processes.

- Open surface mount solder joints have been found after a period in service. These "cold" or "dry" solder joints were characterized by a component termination and substrate land which were mechanically touching but not completed with a permanent solder connection with intermetallic compound (IMC) formation can open during service. Tin-lead to tin-lead mechanical contacts (under light mechanical loading and not soldered) oxidize and open in service under temperature cycling or vibration/shock conditions. This failure mode is similar to the "fretting corrosion" described in these appendices.

Failed joints have been traced to

- planarity (or coplanarity) problems on the component termination
- planarity (or coplanarity) problems on the substrate land
- solderability problems on the component termination and on the substrate land
- improper selection of solder paste/flux.
- improper solder reflow processing.

Difficulty in inspection has resulted in "dry" solder joints that are seen on J-lead solder joints. These "dry" joints are insidious because they can be intermittent and be reported as "NTF;" however, gull-wing terminations are not exempt. Gull-wing leads are preferable to J-leads only because they are not hidden under the component and solder joints can be inspected and reworked more easily. Some solder joints to gull-wing terminations have been found to be open due to excessive IMC formation and mechanical disturbance during solder solidification. Some companies use an electric or air driven plunger to "tap" PWAs during functional test to detect "cold" or "dry" solder joints. Some repair technicians use a pencil "tapper" to detect these solder joints. "3D" optical or X-Ray systems may be fast enough and definitive in their detection of defective joints.

- for the ideal SM solder joint of uniform thickness (for minimum dispersion in the Nf or cycles to failure), the surface of the solder paste on the lands of the printed board must be coplanar (in the same plane), all the leads of the SMT component must also be coplanar and contact the solder paste simultaneously. If there is a gap between any lead and the solder paste, a defective joint is likely.

Coplanarity and solder volume issues include:

- Maintenance of component lead coplanarity requires appropriate shipping and storage containers, such as trays rather than tubes for Ceramic Leaded Chip Carriers to prevent lead interlocking and damage and storage of parts to be used for repair/rework or "kitting" in the original container rather than loosely "binning" them,
- Some of the requirement for perfect coplanarity is alleviated because the component leads sink into the solder paste and into the molten solder; this requires that cumulative coplanarity (between the substrate and the component leads) apply over the dimension of the component to ~100 μm. Solder paste thickness for Fine Pitch and extra Fine Pitch (FP, XFP) is less than that for the coarser pitch of 0.5 - 1.2 mm components and therefore the cumulative coplanarity requirement is tightened to ~75 μm, again over the dimension of the component.

  Large, uninterrupted stencil openings result in thin paste in the middle of the opening; paste uniformity is aided by assembling the large opening from a multiplicity of narrower openings with the long axis parallel to squeegee blade travel.
- Planarity of the substrate lands is lost, particularly in the case of Fine Pitch and extra Fine Pitch (FP, XFP), when the substrate is processed through hot air solder leveling or hot air leveling (HASL or HAL). These processes leave uneven deposits of solder on the pads with the distribution often a function of the location of the pad on the panel.
- The volume of solder in the joints can be reduced by via and feedthrough holes/pads, as well as large area conductors or other large lands very close to components lead pads; these features tend to draw solder away from (steal or thieve) the intended solder joint and should be covered with solder mask or separated with narrow conductors, covered or not with solder mask. The presence of a large number of solder balls or a number of large solder balls also indicates a reduction in the solder available for joints.
- The ideal SM solder joint is metallurgically joined to the component lead and to the substrate land with no voids in the joint nor sign of non-wetting or dewetting

of the solder. The conditions require that the termination finish and the lands be solderable, the solder paste/flux is sufficiently active with no moisture in the paste during reflow, and the reflow conditions be well specified and executed.

- The large number of small, narrow, closely spaced leads on a given component does not allow the evaluation or measurement of the component lead solderability; often, the production reflow operation demonstrates the marginal solderability of the termination finish on one (1) lead of one component with 68 leads. Similarly, the large number of very small pads on a given printed board does not allow the evaluation of the solderability of the printed board. Some PWAs fail because of one (1) failed joint out of several thousand. Confounded with component termination solderability is the preferential wetting of the termination by the flux and molten solder when soldering temperature is achieved by the termination before the land.
- Repeated HAL or HASL (hot air solder leveling) processing of the printed board can result in exposed copper-tin IMC which rapidly oxidizes and has extremely poor solderability.
- The move to "low residue," "leave on" or "no-clean" flux technologies results in fluxes which are milder and less able to penetrate oxidized termination and land finishes.
- The effectiveness of the solder paste is sensitive to many factors such as mean solder particle size, particle size distribution (particularly the fines content), oxide content of the solder particles, moisture content of the flux vehicle (as manufactured or after any subsequent exposure to moist air). The SM process, if not properly controlled, can exacerbate the degradation of the paste through such process deviations as excessive drying (loss of tackiness) prior to placement of SM components, re-use of paste from day to day, or opening of the paste jar without proper warming of the contents to room temperature. Insufficient preheating prior to reflow can result in inadequate activation of the flux while excessive or prolonged preheating prior to reflow can result in oxidation of the solder metal particles and exhaustion of the flux. Many of these factors contribute to solder balling.

  Solder balls are reported to result in short circuits by bridging component pads of an MLCC connected to Vcc and Gnd, resulting in a charred printed board. Solder balls can be the result of improper handling and processing of the solder paste or the injection of solder through a via or PTH. The one or more solder joints on the PWA may lack the solder in the balls and solder joint reliability may be compromised.
- Some joints may not achieve the required temperature for correct solder reflow under infrared (IR) conditions because of the differences in thermal mass of components (such as high pin count connectors or sockets and those PGAs with affixed heatsinks), thermal shadowing effects from overhanging portions of taller components and the component leads termination finish; similarly, to avoid the heat sinking effects of ground and power planes, component lead connections to power and ground planes should be made using thermal relief (isolated) pads connected to the larger planes by thin conductors. Conductors to fine pitch land patterns also have solder thieving and heat sinking effects during the reflow process.
- Formation of excessive brittle copper-tin IMC at temperatures encountered in SM processes, including rework/repair degrades the ability of the solder joint to withstand temperature cycles. Photographs of these IMCs are in Solder Joint Reliability and in Metallurgy of Solder Joints in Electronics; Scanning Electron Microscope (SEM) photographs of solder joints are in Soldering in SMT Technology.
- Solder joints are subjected to thermo-mechanical stress during cool down after mass reflow soldering where the entire printed board is heated; this effect is exacerbated where the design includes components which are long, stiff, or possess a low coefficient of thermal expansion (CTE). Examples of these components include RFI fences, ground bars, power/ground/filter distribution laminates, and board stiffeners. Variation of the time at temperature during reflow will be reflected in the incidence rate of failed joints due to the stress arising from cool-down. The cool-down phase of the process can cause warping of printed boards or can flex warped boards such that solder joints and components are stressed and broken; stresses may be reduced if stress relief bends and curves are designed into the part. A long, heavily filled SM connector which is not mechanically restrained and in which the contact inserts are captured may fall into this category. Hot bar reflow at AT&T of 600 pin connectors, laser soldering, single point TAB bonding and scanned light energy sources have been used to address the issue of heating the entire printed board.

  Note that a 4-sided "box" of rigid components such as a complete RFI fence will be robust with respect to mechanical flexure but will result in a "z" axis flexure in the center of the "box" during SM reflow and subsequent thermo-mechanical solder joint stress upon cool down.

The hard, brittle IMCs embedded in the much softer solder matrix require changes to the metallurgical sawing/polishing/etching techniques normally used for homogeneous materials.

The solder joint quality is dependent on the volume of solder present. Typically, a stencil or screen will be used to deposit the proper volume of solder paste. While the performance range of the various SMT processes vary, studies have shown that over 63% of defects identified after reflow originate during the solder paste screening (or stenciling) step. Correct solder paste volume is controlled by the stencil or screen emulsion) thickness, aperture opening size, solder mask height and stencil process parameters (such as squeegee hardness and pressure).

While either stencils or screens may be used for surface mount leaded parts of 1.2 mm pitch and greater, stencils are preferable for fine-pitch work. Although stencils cost more and require longer lead times for construction, they clog less frequently, and provide longer wear life and a greater degree of control.

The challenge for the screen or stencil designer is to provide for the correct volume of solder paste to the corresponding land area while preventing bridges caused by excessively wide apertures. Actual aperture sizes and stencil thicknesses must be determined from solder volume calculations or experimentally to suit the paste type, board, tinning thickness and inspection expectations.

If the surface mount assembly contains a mix of various pitch packages on the same board, it will be necessary to engineer a stencil which can deposit various amounts of solder without compromising the integrity of any component's attachments. There are at least four alternatives in this situation:

(1) step-down stencils which have a thinner foil thickness in the fine-pitch land areas

(2) stencils which have the land apertures reduced in only the fine-pitch areas

(3) modified land stencils which have aperture openings on alternating ends of the fine-pitch lands and

(4) stencils which use fancy shaped apertures (such as tear-drops, triangles, etc.).

The option chosen must be based upon design, as well as manufacturing considerations.

Appendix N
Adhesives, Solder Mask and Conformal/Other Coatings

N-1.0 ADHESIVES

Moisture and Adhesion The molding compounds used to encapsulate SM electronic components are reported to decrease slightly in the value of Tg and to lose adhesion to the other materials in the assembly with increased moisture weight gain. Older anhydride cured epoxies suffered from "reversion" or the chemisorption of water and the subsequent conversion of epoxide ring to carboxylic acid.

N-1.1 Electrically Conductive Attachment Materials Permanent interconnections include metal and carbon particles in thermosetting adhesive or thermoplastic adhesive matrices. The metals include silver, nickel, silver-plated nickel, copper, silver-plated copper, gold, silver-plated glass spheres. The thermosetting adhesives include epoxy, polyimide and bismaleimide resin systems. The thermoplastic adhesives include acrylics.

Electrically conductive attachment materials include epoxy, polyimide and bismaleimide polymers containing metal particles of silver, gold, nickel, copper, silver-plated nickel, silver-plated copper, and silver-plated glass spheres. Some of these systems are 100% solids and require only heat to cure. Others contain some solvents to reduce the viscosity and require a drying phase prior to cure. These materials may also be used as thermal conductors, if electrical isolation is not required.

A reliability concern with conductive adhesives is the loss of conductivity at the interface between a cured rigid filled epoxy and a reflowable metal termination finish such as tin-lead solder when the assembly is exposed to temperatures approaching the melting temperature, Tm, of the solder. The movement of the solder away from the rigid epoxy adhesion interface can lead to an increased electrical resistance.

A moisture-related concern is the loss of electrical conductivity at the interface between a metal filled epoxy and a metal termination finish other than of silver or gold; tin, lead, and nickel oxides formed as a result of moisture permeating the epoxy are not highly conductive and lead to an increase in interfacial electrical resistance with time.

N-1.2 Thermally Conductive Adhesives Thermally conductive attachment materials include epoxy polymers containing such fillers as alumina, cubic boron nitride, and zinc oxide. The function of this class of materials is to fill the void or space between the power dissipating component and the heat dissipater. Thermally conductive materials which are not attachment materials include lands, tapes and stamped shapes of elastomeric materials either filled with alumina, cubic boron nitride, or zinc oxide or laminated to aluminum or copper films; these forms require that mechanical pressure be applied between the component and the heat dissipater.

N-1.3 Mechanical Attachment Adhesives Mechanical attachment adhesives include SM adhesives intended to secure the component during wave solder, or to secure the component while it is hanging upside down on the substrate through a reflow operation, or to secure such components as crystals in service. These materials include very thick resin or rosin flux, and epoxy or acrylic polymers (cured by UV, heat, or anaerobically) and hot melt glues.

N-2.0 SOLDER MASK

Solder mask is a thin polymer coating that is applied to the surface of printed boards during fabrication. Due to its nature, solder mask is often used to protect areas of the printed board from environmental effects caused by dust, moisture and contamination. The capability of a solder mask to insulate and protect the assembled board is essential to reliability. The pertinent performance and qualification requirements for solder mask are defined in IPC-SM-840 which covers the range of mechanical, chemical and electrical properties which a solder mask must possess. However, a "pads-only" approach also achieves these goals and has many other advantages that should be considered.

Solder masks provide a variety of functions when applied to selective areas of the printed board. In addition to providing a thermal and electrical insulation layer, solder mask prevents the formation of bridging during soldering processes and reduces weight gain due to solder. Whether or not solder mask is necessary for a particular design may be based on many factors.

Many multilayer military and space applications use a "pads-only" outer layer design. By submerging all conductors and power planes in the innerlayers, only the land areas are exposed on the board surface. Connection to the sublayers is then accomplished by small plated and filled vias inside the land area. If a "pads-only" approach is not feasible, then it is crucial that solder mask be applied for surface mount designs to act as a dam to solder migration.

"Pads-only" approach has several advantages worth noting:

- The "pads-only" construction is compatible with soldering processes, conformal coatings and common cleaning solvents.
- The electrical and dielectric performance of the pads-only construction is no different than the remainder of

the PWA. Stenciling of solder paste is improved with a "pads-only" approach.

- Application of solder mask to flexible and flex-rigid PWAs may be difficult.
- Resolution of the "pads-only" approach is the same as the resolution of copper etching.

The solder mask material system must be compatible with the soldering process and its materials (temperature, duration of exposure, flux, cleaning solvents); exposure to heat and chemicals changes the reactivity and morphology of the surface and can lead to adsorbed flux residues and to degraded SIR. Some laminates such as polyimide (and some laminate reinforcement materials such as aramides) absorb sufficient atmospheric moisture that the printed board should be thoroughly dried prior to reflow; otherwise delamination between the solder mask and the printed board (or between the reinforcement and the resin) may occur.

The solder mask material system must be compatible with the other assembly processes such as marking, bonding and component rework/repair (re-soldering) processes (temperature, duration of exposure, flux, cleaning solvents). High printed board temperatures after exposure to moist atmospheres may result in delamination at the solder mask-printed board interface. High printed board temperatures for long durations can result in thermal degradation of the solder mask as well as measling of the base laminate. (See IPC-R-700.)

Solder mask may be dissolved or degraded by the solvent or material system in the conformal coating. Problems may be avoided by informing each intended supplier of the solder mask-conformal coating materials expected to be used and of the service environment for which protection is required before the material systems of the product have been decided.

Open or untented PTHs and PTVs (no solder mask on either side of the printed board) can allow liquid flux to be trapped with potential for corrosion, reduced SIR, contaminated test fixtures and causing electrochemical corrosion. (See IPC-D-275.) If solder mask is intended to plug or tent these holes, it must do it consistently. Another method to prevent flux from being trapped in these vias is to plug them with solder (which wave soldering does automatically).

Solder mask overlap onto the land pattern (whether by design or by loss of process control) resulting in solder joint area reduction and reduced solder joint reliability. (See IPC-D-275, IPC-SM-782, and IPC-SM-785.)

Solder mask overlap onto or residue on test lands (whether by design or by loss of process control) reduces test reliability. (See IPC-D-275 and IPC-SM-782.)

Solder masks are not recommended for application over solder coated conductor surfaces. The solder melts or reflows during subsequent processing (particularly hot air solder leveling or wave soldering); delamination at the solder mask/metal interface may allow contaminants to become entrapped. If solder mask is required over solder, cross-hatching is recommended for those conductors which exceed specific dimensions.

The robustness of solder masks' ability to minimize copper corrosion in the presence of such chemicals as the polyglycols appears to depend upon material system, DC voltage level and user process. Polyglycols are found in fluxes used with aqueous cleaning processes and in fusing fluids used with hot air solder leveling. Some solder masks may exhibit cracks after exposure to low temperatures.

Design Requirements and Considerations Proper solder mask design is essential to the construction of a reliable surface mount assembly. The ideal solder mask design covers all the circuits and leaves all lands and surface mount pads completely free to facilitate the formation of solder joints. Solder mask design must evolve from interaction between the board designers, printed board fabricators and assembly manufacturers. Good solder mask design results from the definition of clear final product requirements based upon the desired level of reliability and the impact of board fabrication and assembly capabilities. Once these issues are addressed, a concise set of design rules can be formulated and tested.

N-2.1 Types of Solder Masks There is a broad range of available solder masks, most of which can be categorized into three types: liquid screenprinted, dry film and liquid photoimageable. Each type uses a different method of application and produces a unique combination of advantages and disadvantages.

N-2.1.1 Liquid Screenprinted Solder Mask Liquid solder mask is applied by screen printing through a mesh containing a blocking emulsion in areas where the material is not required on the finished board. This is the original type of solder mask and provides the lowest cost alternative. Thickness of this type of mask is a direct result of the screen emulsion thickness and can typically reach up to 50 µm. While tenting of holes with this solder mask is not possible, vias can be reliably plugged for holes of up to 1.1 mm with a properly designed screen printing process. Due to registration limitations and bleedout, liquid screen-printed solder mask is usually not acceptable for high density surface mount applications.

N-2.1.2 Dry Film Dry film solder mask starts as a pliable sheet of photosensitive material of a specified thickness (commonly ranging from 75 to 100 µm). By using a combination of heat and vacuum, the lamination process ensures encapsulation of board circuitry. Subsequent processing through exposure to UV light and development to

remove mask from clearance areas, results in the final coverage. Dry film is the high cost choice; however, it has several advantages over liquid screenprinted masks. It can provide not only reliable tent vias but can also provide a relatively thick, uniform coating with superior registration and resolution. These features are especially useful in the case of vias placed under low clearance components or where impedance-controlled circuitry is present on the external layers. It does have the distinct disadvantage of resulting in a solder mask that extends higher than the lands it surrounds. This relative geometry translates directly into increased defects for surface mount joints during the wave and reflow soldering processes. Where tenting of via holes is not required, dry film solder mask can be difficult to remove from holes smaller than 0.5 mm and may affect solderability in these areas.

Some dry film solder masks (in combination with particular solder fluxes) appear to increase the incidence of solder balls, reducing the effective conductor spacing. This may increase the risk of corrosion and reduce the reliability. Solder balls reduce the solder in the attachments and may reduce the fatigue life.

Cracked and flaking dry film solder mask may be the result of thermal abuse or overcure; solder mask tented over PTH and vias may crack and entrap liquid flux. The flux may leak out and contaminate testing fixtures; corrode the barrel of the PTH or PTV; and contribute to the growth of metallic dendrites or conductive anodic filaments. (See IPC-TR-476 as well as Design for Testability.)

In direct response to these high defect levels, solder mask suppliers have developed alternative dry film processes to address the unique needs of Surface Mount Technology. The first is a thinner solder mask 60 µm which utilizes an additional process after hot roll lamination to ensure complete encapsulation of the circuitry with the reduced thickness needed for high soldering yields. The size of via holes which can be tented with this thinner mask is limited to about 0.6 mm, however, this new method provides a superior combination of features necessary for surface mount assemblies. The second method uses a liquid photopolymer underneath a thinner dry film layer to help bridge the circuits and fill the via holes to support the solder mask tent. This results in a total mask which is about 50 µm thick. Since the via holes are completely filled with the photopolymer, it is critical that the bare board fabricator completely cure this type of solder mask. Without a complete cure, outgassing during subsequent soldering processes will lift the tents as volatiles in the vias escape during these thermal excursions. Some users have noted that this "combination" mask increases in thickness around the SM lands (up to 125 µm), thereby negating the advantage of using a thinner solder mask.

N-2.1.3 Liquid Photoimageable Liquid photoimageable solder masks are the most recent group of solder masks to be developed. They provide a lower cost alternative to dry films where the tenting (or filling of via holes) is not required. These materials can be applied to the printed board by a variety of methods which include: open screening, curtain and roller coating or by electrostatic spraying. Following subsequent photoimaging and development, photoimageable solder mask provides very high feature resolution. Combined with the fact that this solder mask application is only 15 to 30 µm thick, it provides excellent resolution where small features are required (such as between lands for fine-pitch components).

Designs which minimize flux entrapment are permitted by solder mask systems which combine application of dry film and liquid film solder mask materials; these composite systems may result in solder mask on and local thick ridges around the land patterns and test lands.

N-3.0 TEMPORARY MASKS AND STOPS

Temporary coatings, tapes and solder masks can be used to prevent damage to connectors, variable components and switches by solder, flux, cleaning solvents, and conformal coating. In SMT, the barrier may have to withstand very high process temperatures as well as very high solvent spray pressures. The solvent damage to the components includes corrosion, metallic dendrites, and loss of lubrication. In some cases, loss of the solder mask has plugged the cleaning system plumbing.

Some temporary removable solder masks containing NH_4^+ can corrode base metals or contribute to galvanic corrosion at exposed interfaces of dissimilar metals; residues from this class of solder mask may also inhibit the cure of silicone conformal coatings which are catalyzed by platinum compounds. Other, removable masks decrease in their "removability" after exposure to high processing temperatures.

Some temporary solder masks soluble in organic solvents react chemically with flux vehicle components during the soldering process; the reaction products may be detrimental to reliability. The residues from this class of solder mask may trap flux and flux residues, leading to later corrosion. It is critical that the temporary solder mask leave no residue. If a residue remains which is not cleaned off, it may interfere with contact mating, solderability, or conformal coating.

N-4.0 CONFORMAL COATING

The primary purpose of conformal coating is to provide environmental protection for the electronic assembly. Conformal coatings are polymeric materials which may be as thick as 250 µm thick.

Conformal coatings provide environmental protection by keeping contaminates from the circuits and adhering to the

surface to prevent moisture from collecting. All conformal coatings are permeable to moisture. The key issue is to prevent the moisture from collecting at an interface between adjacent conductors. Moisture will collect at an interface if there is a loss of adhesion due to: a) thermal stresses or b) the presence of contaminates which will trap moisture. As contaminates trap moisture they vesicate the coating providing a gap for corrosion to form. Moisture, coupled with contamination to increase the conductivity, creates an electrolytic cell between conductors which results in corrosion. Conformal coating also prevents shorts of adjacent conductors by loose metal fragments.

N-4.1 Selection of Coating Selection of conformal coating depends on the use environment, the design of the electronic enclosure, and the manufacturing facilities available. In the worst environment, exposure to saltwater and temperature cycling, the assembly may require potting or encapsulation instead of conformal coating to be reliable. The use environment needs to be understood in terms of the temperature range, exposure to corrosives, chemicals and solvents, and permissible outgassing. The design of the enclosure also has an effect. An enclosure which is cooled by fan drawing air from the outside is different than an enclosure which is sealed or purged with dry nitrogen.

Some conformal coatings have been formulated to be cured rapidly with ultra-violet light; in some cases a secondary heat cure may be required.

N-4.2 Thermal Stress Design Considerations Thermal cycling may cause a number of problems with conformal coating. If the coating fills the gap beneath a component which does not have sufficient stress relief in the leads, the stresses, generated by the temperature excursions and a mismatch in the coefficients of thermal expansion, may fatigue the solder joints and result in solder joint failure. Hard coatings like epoxy may apply excessive stresses to glass bodied components and can crack them. Some coatings like polyurethanes and silicones may be soft at room temperature, but if they are cooled below the glass transition temperature, their elastic modulus may increase several orders of magnitude. This may generate excessive stresses like epoxies coatings. These stresses may be minimized by selecting a coating with a T_g lower than the lowest exposure temperature and applying the coating in the proper thickness. (Each coating has a recommended thickness.)

Obtain the information on CTE, Modulus and T_g from the conformal coating supplier. Examine the design with this information in mind.

Before application or re-application of any conformal coating, the surface of the PWA and the components must be free of materials (water soluble, ionic contaminants, greasy, oily or particulate), which might interfere with wetting, or trap moisture; otherwise, mealing or vesication will occur with subsequent corrosion and dendrite formation between adjacent conductors.

N-4.3 Chemical Stress Design Considerations Some coatings are not stable in hot, humid conditions and may revert to a gel. Select reversion resistant polyurethanes. Parylene coating will be attacked by oxygen and crack if exposed for extended periods at temperatures above 125°C. Silicones are attacked by some solvents; in addition, traces of silicone may interfere with subsequent bonding and painting operations. Acrylic conformal coatings are removed by most cleaning solvents including alcohol. Do not select acrylic coating where solvent resistance is required.

N-4.4 Space Environment Design Considerations Some conformal coatings outgas significantly, making them unsuitable for spacecraft. Fluorescent chemicals added to the conformal coating outgas and may cause problems where optical clarity is paramount in systems with lenses, mirrors and viewing ports.

N-4.5 Manufacturing Considerations There are several key steps in applying conformal coating, the most important being the cleanliness. An ionograph, although useful for process control, is not sufficiently sensitive to detect a level of ionic contamination which will cause vesication (blistering). Non-ionic contaminates, such as silicone, will interfere with adhesion of epoxy and polyurethane conformal coatings. The cleaning process should include cleaning with both polar and non-polar solvents. Other process controls should include proper mixing, application and curing of the coating.

The conformal coating may contain solvents which affect the adhesion or integrity of component and printed board markings, labels and legends.

Conformal coating of PWAs fabricated on fluorinated plastics will require pre-treatment to improve adherence to the substrate. The coating will increase the effective dielectric constant between surface conductors (reduce high frequency performance).

N-4.6 Other Design Considerations Conformal coating on test pads results in diminished test accessibility; testability buss methodologies and structures may be required to permit effective and efficient fault coverage. (See IPC-SM-782.)

Reduced heat extraction from the PWA (and increased junction temperatures) may result if conformal coating covers heat sinks such as card edge clamps and cold plates.

Where solder coated conductor surfaces are overcoated with rigid CC, the solder melts or reflows during subsequent processing (particularly hot air solder leveling or

wave soldering) and delamination at the conformal coating/metal interface may allow contaminants to become entrapped and blistering of the conformal coating. This may contribute to electrochemical corrosion or migration.

Conformal coating removal must be performed in a manner which:

- provides a mechanically and electrically sound, dry, clean surface to which conformal coating material will be applied;
- minimally degrades the underlying solder mask or its adherence to the printed board. (Some CC removal solvents also attack some solder mask materials; excessive temperature during removal of epoxy or polyparaxylylene CC may degrade the underlying solder mask, or where the solder mask or laminate have absorbed substantial water from the air, may cause delamination of the solder mask from the laminate or delamination within the laminate);
- minimally degrades the surrounding conformal coating or its adherence to the printed board. (CC removal solvents do not remain on the surface but can permeate the CC film and may affect the CC- solder mask interface; CC removal solvent residue if not effectively removed may lead to latent corrosion failures; thermal removal of epoxy coatings with soldering iron, hot air or laser, can char or otherwise degrade the surrounding area. Mechanical abrading techniques can be used to remove CCs and solder mask and to remove thermally damaged coatings if ESD damage is not a concern);
- does not degrade or contaminate components which are to remain in place. (CC removal solvents may contain corrosive, polar or ionic materials and can attack the polymers of which components are made; solvent stress cracking may develop in the long term. See IPC-R-700.)

Conformal coating rework or repair must be performed in a manner which restores the functionality of the coating with respect to adherence to the printed board and components and with respect to freedom from delamination, voids, and inclusions. (See IPC-R-700.)

N-5.0 COMMON CRITICAL PROPERTIES OF SOLDER MASK AND CONFORMAL COATINGS

Conformal Coatings:

- Provide mechanical protection for the surface mount (SM) PWA during assembly, test and service;
- Provide a smooth, chemically stable surface to reduce SM PWA susceptibility to effects of condensing atmosphere and electrochemical corrosion/migration during test and service;
- Permeable to water vapor

CCs are dependent upon these factors for effective performance under humid conditions:

- a clean underlying substrate surface free of water soluble materials prior to application (to prevent mealing, vesication, growth of metallic dendrites). Non-polar solvents do not effectively remove these soils;
- a clean underlying substrate surface free of solvent, greasy, oily, particulate and other materials which interfere with adhesion of the film (to prevent delamination and growth of metallic dendrites). Polar solvents or water without detergents do not effectively remove these soils. Additional, ultrasonic energy may be required to remove and suspend particulates as well as contaminants in cracks and crevices (see IPC-CH-65);
- a dry substrate free of excess moisture and solvents (whose vaporization during exposure to the heat of assembly processes may result in delamination of the coating from the substrate);
- complete encapsulation of conductors - film formation with no voids bridging conductors and no voids along conductor edges;
- mutual compatibility of solder mask and conformal coating where both are used;
- a proper cure for a strong, coherent film free of cracks, voids and inclusions. (See IPC-S-816, IPC-PE-740.)

Some cleaning solvents such as chlorinated hydrocarbons and alcohols attack or swell some solder mask formulations and some conformal coatings.

Leaking capacitor electrolytes such as sulfuric acid, dimethyl formamide, and gamma butyrolactone, particularly at high use temperatures may degrade some coatings; these electrolytes are also used to remove conformal coatings.

Liquid flux entrapment in PTHs and PTVs may be minimized by the selective deposition in and filling of the barrels with liquid solder mask material or liquid conformal coating material. Filling of the barrels with liquid solder also accomplishes the same purpose.

Solder joint reliability under temperature cycling or power cycling conditions may be reduced if the solder mask touches the bottom of the component or conformal coating filling the printed board - component gap. (See IPC-SM-785.)

Degree of outgassing must be quantified and appropriate, particularly for space applications, where outgassing is a vital concern around optical surfaces such as lenses, mirrors and detector faceplates. Outgassing is also important where unsealed relays, switches or separable connectors are used; micromovement or electrical arcing can form semi-insulating deposits of carbon or silica materials on the contacts.

N-6.0 JUNCTION COATINGS, "GLOB-TOPS"

A specialized category of coatings includes the semiconductor junction, chip or die coatings such as the screen printed epoxies or polyimides, spun on polyimides, and chemically vapor deposited poly-paraxylylene which are deposited on the chip in wafer form and patterned; "glob-top" epoxies and silicones which are deposited on the interconnected chip; chemically vapor deposited poly-paraxylylene which are deposited on the chip and wire-bonds, unpatterned; and special purpose pyrolized silicones. The application of junction coating material over contamination creates a corrosion timebomb.

Junction coatings are intended to provide:

- Mechanical environment protection from scratches of the chip surface and disturbance of interconnections.
- "Reliability without hermeticity" by excluding liquid water and by limiting halide and alkali metal content to very low levels under hot water extraction conditions.
- Low stress upon cool down, where the coating is cured.
- In some cases, protection for DRAMs from alpha particle upset.
- In the case of poly-paraxylylene, increased bond wire strength.
- In some cases, "planarization" of the chip surface in preparation for encapsulation by thermoset molding.

Junction coatings may also introduce additional reliability concerns such as:

- Shear stress on the surface of the chip during cool down.
- Compressive stress on conductors on the chip surface, increasing possibility of hillocks and voids.
- Shear stress on ball bonds during temperature cycling with the junction coating is about as thick as the bond is high.

Appendix O
Aerospace and High Altitude Concerns

O-1.0 INTRODUCTION

Use of Surface Mount Technology for aerospace and high altitude applications has the same problems that are experienced with through-hole technology. The problems are as follows:

- lack of air for convection cooling
- larger thermal excursions
- contamination
- radiation environment
- change in dielectric property of gases with pressure
- lessened gravitation or pseudo-gravitational effects.

The degree which these problems impact the design of surface mount assemblies depends on the precise space environment, the purpose of the mission, and the system design. A detailed analysis may be needed for each PWA to determine the extent of the problems.

O-2.0 THERMAL DESIGN

At sea level, natural or forced air convection greatly assists in the cooling of electronic components; however in un-pressurized compartments, there is little or no air for convection and additional thermal considerations must be made. Since radiation is negligible at the temperature of interest for most SM PWA the only way to remove heat is by conduction. Many components generate heat which requires dissipation to prevent excessive junction temperature; heat removal may be enhanced with thermal materials placed beneath these components. However, the thermal material placement must not result in excessive thermo-mechanical stress on the solder joint and subsequent solder joint failure by fatigue when the assembly is thermally cycled. Simulation, analysis and testing is needed to determine the thermal control measures needed for components and SM PWA in space.

O-3.0 LARGE THERMAL EXCURSIONS

In addition to the normal thermal issues in packaging design, the space environment adds a new consideration; thermal excursions due to the effect of the sun/shade exposure. While exterior surfaces of the spacecraft may be exposed to 100,000 temperature cycles from –60 to +120°C, through temperature control, the temperature of internal regions of the satellite may be limited to a few temperature cycles of 5°C. In a deep space mission, the temperature may be as low as –270°C. These differences are critical in the selection and use of materials and a systems level as well as a PWA level, thermal analysis is critical in designing electronic packaging.

The following are a few general guidelines in selecting materials for wide temperature extremes:

- Exercise caution in using polymeric materials with glass transition temperatures (T_g) in the temperature range of test or use. Material properties change rapidly and drastically near T_g.
- Ensure compliant joints and bond lines between materials with different coefficients of thermal expansion. Thermally induced stresses may be very large and cause solder fatigue failures, adhesive bond failures, crack ceramic and glass materials or permanently deform metal. Thermal stresses may also be generated if there are large, although perhaps transient, thermal gradients from one part to another or within an individual part.
- Ensure that metals do not undergo a phase change or a change of the heat treatment in the temperature range of interest.
- Ensure that polymers do not crystallize in the temperature range of interest.

Space applications exposed to severe environments require packages robust to temperatures in the –55°C to +125°C range. Hermetic packages may be required to be robust to life cycle environment which include high relative humidity; under extreme levels of shock and vibration, hermetic packages (with flying internal leads) are less robust than plastic encapsulated packages.

O-4.0 CONTAMINATION

Contamination in spacecraft comes in two forms, particulate and condensed outgassed vapor. Particulate contamination may create false stars around the spacecraft by reflecting sunlight causing problems with scientific and navigational equipment. For some spacecraft missions, condensed outgassed vapor is a minor concern; for others, even a monolayer of condensed outgassed vapor is excessive. Condensed outgassed vapor can cloud optical surfaces causing decreased reflectance of mirrors, degraded clarity of lenses and reduced solar cell output with subsequent degraded star tracking capability, possible false data from spectrum analyzers, and other degraded performance in optical equipment. The outgassing species of most concern in a vacuum are compounds which have sufficiently low molecular weight to volatilize from a warm surface and condense on cold surfaces. Gases (oxygen, water, and nitrogen) usually are not a concern because they do not form permanent contaminating films. The worst sources of outgassing material are incompletely reacted monomers and plasticizers found in polymers.

NASA Reference publication 1124 tabulates the results of outgassing tests on many materials. Typical limits on outgassing are 1.0% maximum Total Mass Loss (TML), 0.10% maximum Volatile Condensable Material (VCM). However the maximums vary depending on factors such as spacecraft mission, amount of material used, material location, and thermal/vacuum testing.

Some conformal coatings outgas significantly, making them unsuitable for spacecraft. Fluorescent chemicals added to the conformal coating outgas and may cause problems where optical clarity is paramount in systems with lenses, mirrors and viewing ports.

O-5.0 RADIATION ENVIRONMENT

For some orbits and missions, ionizing radiation concerns play an important design role in component selection and shielding. The primary sources of radiation in space are gamma rays from the sun and trapped radiation in the Van-Allen belt. Radiation has many effects on materials. The most sensitive materials on spacecraft are the exterior thermal control finishes and IC components. The radiation can cause damage to ICs in the following forms:

a. Single Event Phenomena (SEP) which include Single Event Upsets (SEU)
b. Single Event Latchup (SEL)
c. Single Event Gate Rupture (SEGR)
d. Single Event Snapback (SES)
e. Single Event Burnout (SEB) due to Electrical Overstress (EOS)

Analysis is needed to determine if radiation control is required. Radiation control may be accomplished by increasing shielding thickness, selecting radiation hardened components or adding error-correction software. Increasing shielding thickness may be accomplished by increasing the wall thickness of the electronic enclosure or bonding pieces of tantalum sheet to the top and bottom of components.

SEP-related failure rates are expected to increase linearly with the frequency capability of the devices in a system. Protons as well as cosmic rays are implicated in SEP. The earth's proton belt is one region of operation which causes increased SEP rates. Multiple upsets are not uncommon; single error correction schemes are inadequate in these circumstances.

Older radiation-hardened devices are slower and less susceptible to SEP than are such technologies as very high speed, very shallow silicon devices, advanced compound heterostructures such as heterojunction bipolar transistors, and high speed optoelectronic integrated circuits.

O-6.0 ELECTRICAL PROPERTIES OF GASES

Under high or hard vacuum conditions or at "high" gas pressures, the Dielectric Withstanding Voltage (DWV) is higher than at some intermediate pressure. A space-borne or high altitude system tested satisfactorily on the ground may also endure the mission satisfactorily but intermittently fail during the launch phase.

O-7.0 GRAVITY (OR LACK OF)

The effects of gravity are greatly lessened at distance far from massive bodies, such as the earth.

Effects similar to low gravity are found in situations such as geo-synchronous orbit or in forced flight paths used to simulate "weightlessness."

In these circumstances, the orienting effect of gravity is lessened and particles can float around. If the particles are conductive and inside the sealed cavity of an electronic package, the particle may intermittently or permanently bridge conductors, causing failure.

Particle Impact Noise Detection (PIND) evaluation is used with external mechanical excitation (mechanical vibration), to screen hermetic electronic packages for loose internal, possibly conductive, particles to reduce this reliability hazard.

Electrostatic forces may cause the particles to adhere to the surface of the cavity and escape detection.

Appendix P
Technical Acronyms and Abbreviations

ABS* Acrylonitrile Butadiene Styrene
AOI Automatic Optical Inspection
AR Aspect Ratio
ASIC Application Specific Integrated Circuit

BGA Ball Grid Array
CGA Ceramic Grid array
BIST Built-In Self Test
BIT Built-In Test
BITE Built-In Test Equipment
BP Boiling Point

CAD Computer Aided Design
CAE Computer Aided Engineering
CAF Conductive Anodic Filament
CBGA Ceramic Ball Grid Array
CC Conformal Coat(ing)
CCD* Charge Coupled Device
CDR Cumulative Damage Ratio
CFC Chlorofluorocarbon
CIC Copper-Invar-Copper
CLLCC Ceramic Leadless Chip Carrier
CMC Copper-Molybdenum-Copper
CMOS Complementary Metal Oxide Semiconductor
COG* Capacitor Temperature Characteristic
C_p* Process (potential) capability index = USL-LSL/ 6 (estimated process standard deviation)
C_{pk}* Process capability index taking into account two sided specification limits
CPVC* Chlorinated polyvinyl chloride
C-SAM C (-mode) Scanning Acoustic Microscopy
CTE Coefficient of Thermal Expansion
C4* Controlled Collapse Chip Connection
C5* Controlled Collapse Chip Carrier Connection

DAP* Diallyl phthalate
DC Direct Current
DfA Design for Assembly
DfM Design for Manufacturability
DfR Design for Reliability
DfT Design for Testability
DIP Dual In-line Package
DMF Dimethyl Formamide
DMSO* Dimethyl Sulfoxide
DNP* Distance from the Neutral Point
DRAM Dynamic Random Access Memory
DUT Device Under Test
DWV* Dielectric Withstand Voltage

E_a Activation Energy (eV)
EIA Electronic Industries Association
EM Electromagnetic
EMC Electromagnetic Compatibility
EMI Electromagnetic Interference
EOS Electrical Overstress
ESD Electrostatic Discharge
ESDS Electrostatic Discharge Susceptibl (e, ility)
ESR Equivalent Series Resistance
ESS Environmental Stress Screening

FEA Finite Element Analysis
FP Fine Pitch
FR Flame Retardent

GAC Grid Array Components
GBL Gamma Butryolactone
geo geo(-synchronous orbit)

HAL Hot Air (Solder) Leveling
HASL Hot Air Solder Leveling
HAST Highly Accelerated Stress Test(ing)
HCFC Hydrochlorofluorocarbon
HFC* Hydrofluorocarbon

IC Integrated Circuit
ICT In-Circuit Test(ing)
IEC International Electrotechnical Commission
IMC Intermetallic Compound
I/O Input/Output (pins, ports, leads)
IPC The Institute for Interconnecting and Packaging Electronic Circuits
IR Infrared
I_{SB} Current, Secondary Breakdown

JEDEC Joint Electron Devices Engineering Council
JFET Junction Field Effect Transistor
JTAG Joint Test Action Group

KGD Known Good Die

LCC Leaded Chip Carrier
LLCC Leadless Chip Carrier
LDPE* Low Density Polyethylene
LED Light Emitting Diode
leo low earth orbit
LSSD* Level Sensitive Scan Design (M/S F/F design)

MC Moulding Compound
MCM Multi-Chip Module
MELF Metal Electrode Face-Bonded
MGM Molybdenum-Graphite-Molybdenum
MIL-HDBK* Military (US) Handbook
MIL-T* Military (US specifications)
MIR* Moisture Insulation Resistance
MLB Multilayer Board

MLCC	Multilayer Chip Capacitor
MOS	Metal Oxide Semiconductor
MTTF	Mean Time to Failure
NASA*	National Aeronautics and Space Adminstration
NBC*	Nuclear, Biological, Chemical (Warfare)
NF*	Noise Figure
NPO*	Capacitor Temperature Characteristic
NSMD*	Non-Solder Mask Defined
NTF	No Trouble Found
PBGA	Plastic Ball Grid Array
PC*	Polycarbonate
PET*	Polyethylene terephtalate
PGA	Pin Grid Array
PIND*	Particle Inpact Noise Detection
PLA*	Programmable Logic Array
PLCC	Plastic Leaded Chip Carrier
P/P	Pick and Place
PPO*	Polyphenylene Oxide
PS*	Polystyrene
PSMC	Plastic Surface Mount Component
PTFE*	Polytetrafluoroethylene
PTH	Plated Through Hole
PTV	Plated (Through Hole) Vias
PWA	Printed Wiring Assembly
PWB	Printed Wiring Board
PUR*	Polyurethane
PVC*	Polyvinyl chloride
PVDF*	Polyvinyldiene Fluoride
QFD*	Quality Function Deployment
R	Rosin (Flux)
RAM	Random Access Memory
RFI*	Radio Frequency Interference
RH	Relative Humidity
RMA	Rosin, mildly activated
ROM	Read Only Memory
SAW*	Surface Acoustic Wave
SCR*	Silicon Controlled Rectifier
SEB*	Single Event Burnout
SEGR*	Single Event Gate Rupture
SEL*	Single Event Latchup
SEM*	Scanning Electron Microscope
SEP*	Single Event Phenomen(a, on)
SES*	Single Event Snapback
SEU*	Single Event Upset
SIR	Surface Insulation Resistance
SM	Surface Mount, Solder Mask
SMD	Surface Mount Device, Solder Mask Defined
SMT	Surface Mount Technology
SOIC	Small Outline Integrated Circuit (package)
SOT	Small Outline Transistor (package)
TAB	Tape Automated Bonding
T_a*	Ambient Temperature
T_{BL}*	Temperature rise, boundary layer
T_{CA}*	Temperature rise, cooling agent
TCR	Temperature Coefficient of Resistance
TFC*	Thin Film Cracking
T_g	Glass Transition Temperature
TH	Through Hole
T_j	Junction Temperature
T_m*	Melting Temperature
TML*	Total Mass Loss (outgassing)
T_P*	Temperature rise, inside device package
TQFP	Thin Quad Flat Pack(age)
TSOP	Thin Small Outline Package
TTM	Time to Market
T_{TW}	Temperature rise, thermal wake
U/S*	Ultrasonic
UUT*	Unit Under Test
UV	Ultraviolet
VCM*	Volatile Condensible Material
VHSIC*	Very High Speed Integrated Circuit
XFP	Extra Fine Pitch
X7R*	Capacitor Temperature Characteristic
Z5U*	Capacitor Temperature Characteristic